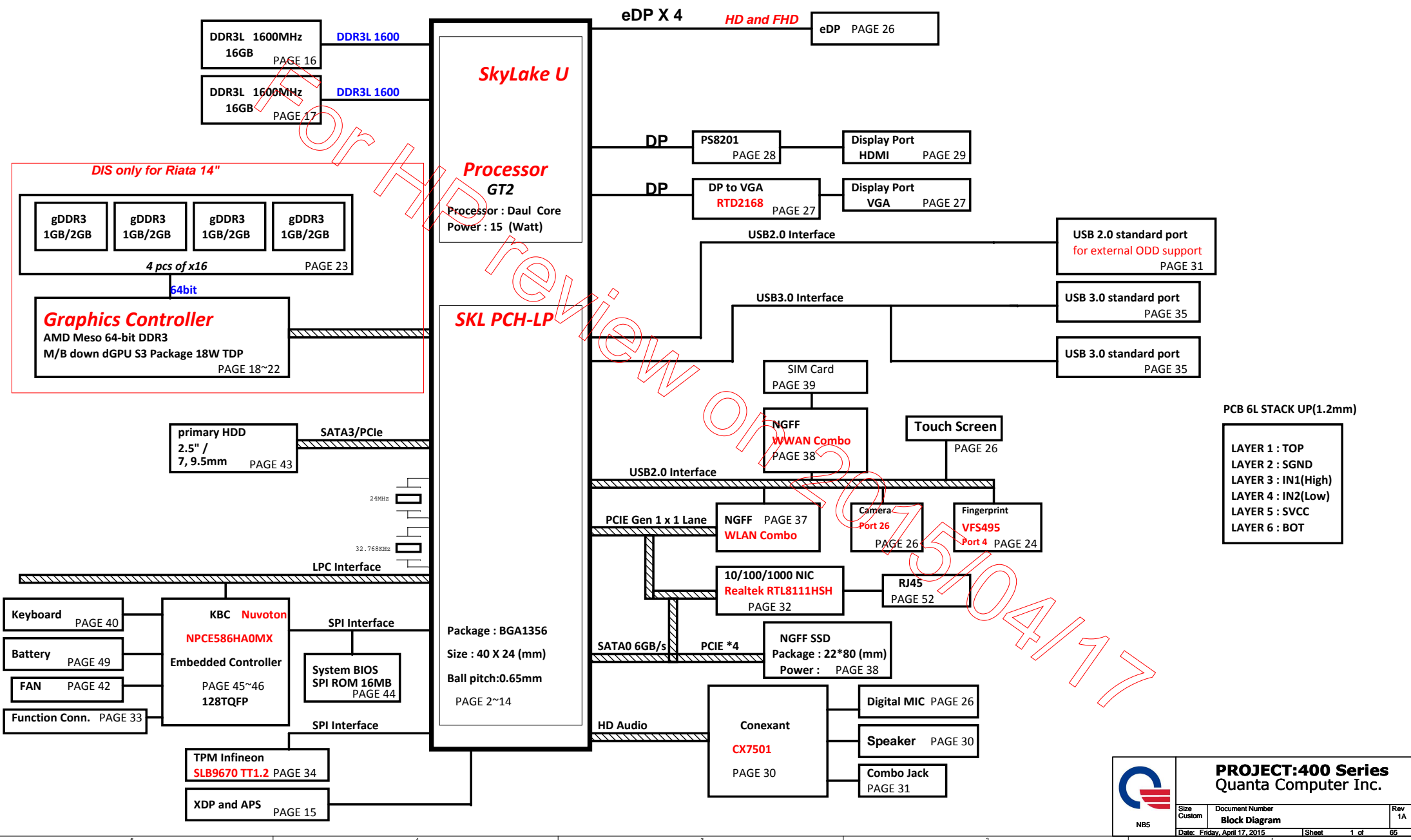
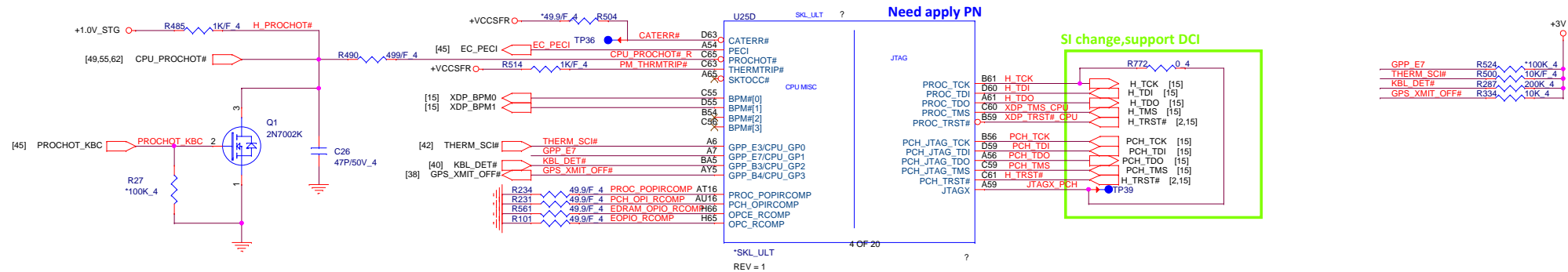


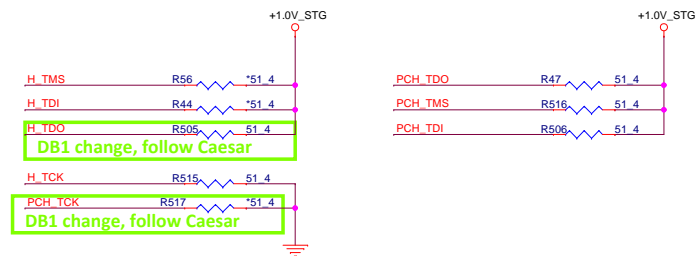
Royal 13"/Riata 14" SkyLake -U (UMA/DIS) Schematics

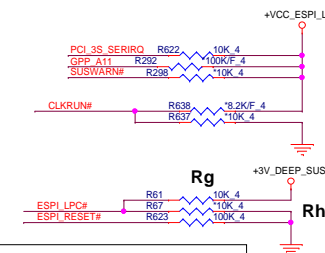
01



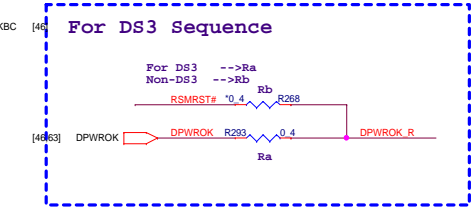
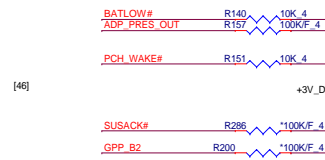


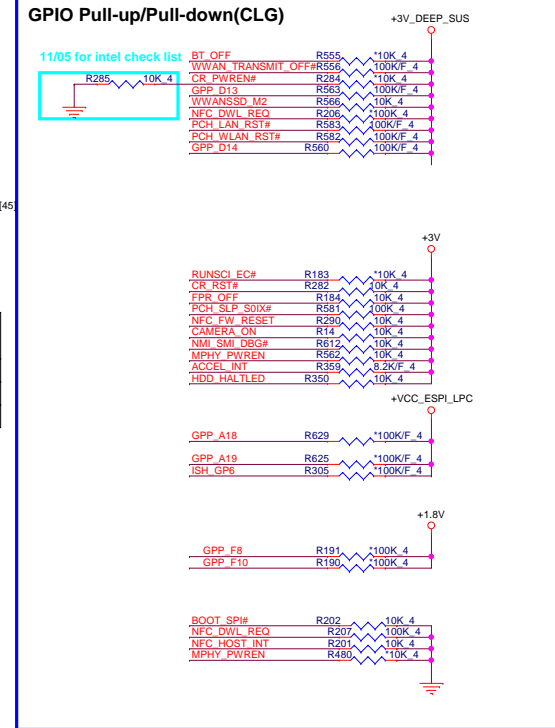
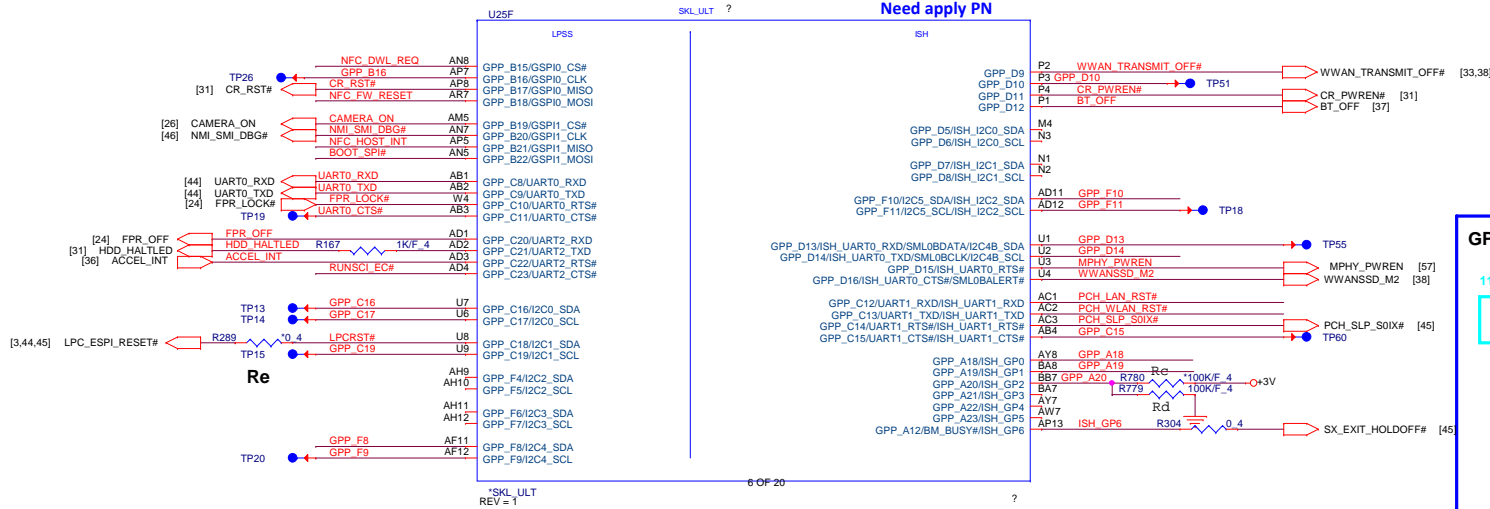
Processor pull-up (CPU)





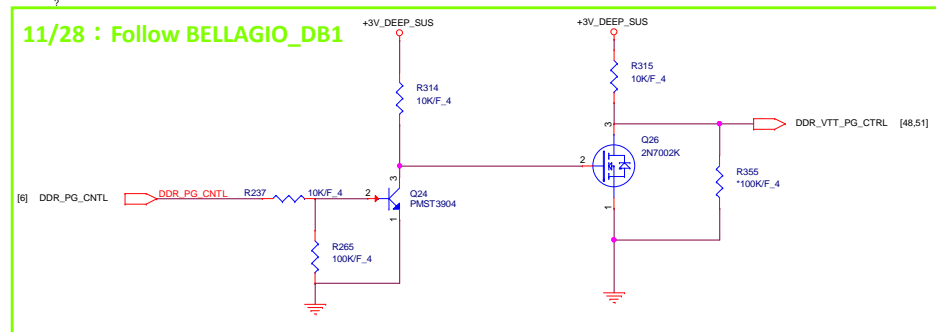
PCH Pull-high/low(CLG)



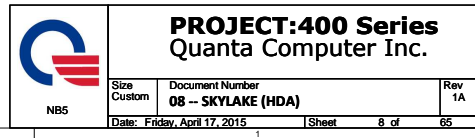


| WWAN & TS TABLE | | |
|-----------------|-----------|----------|
| | WWAN MODE | TS MODE |
| Rc | INSTAL | UNINSTAL |
| Rd | UNINSTAL | INSTAL |

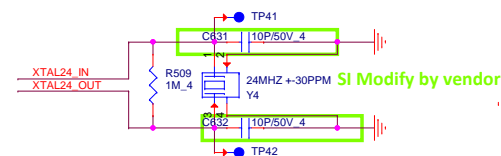
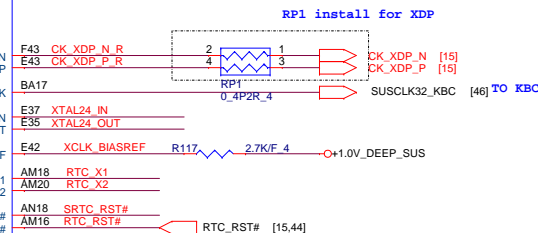
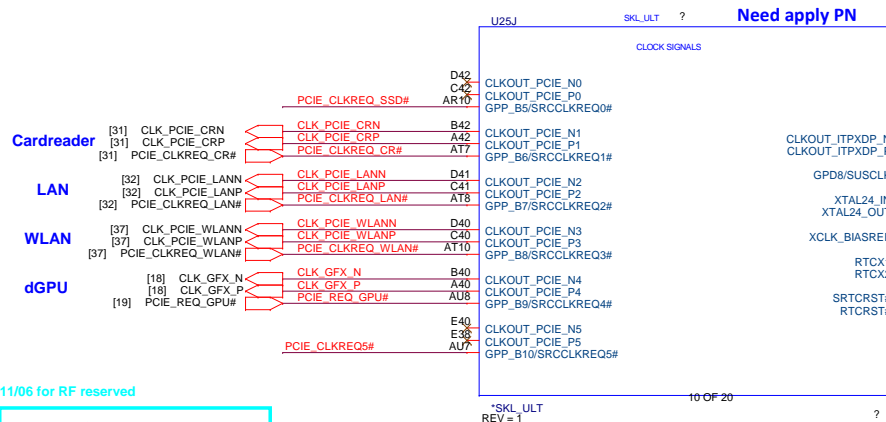
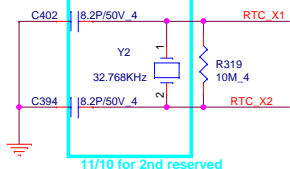
| LPC & ESPI TABLE | | |
|------------------|----------|-----------|
| | LPC MODE | ESPI MODE |
| Ra | UNINSTAL | INSTAL |
| Rb | INSTAL | UNINSTAL |



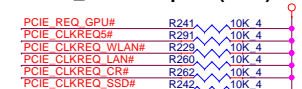




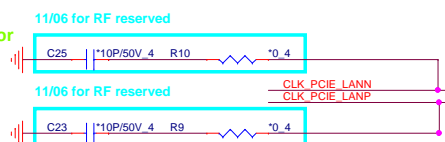
RTC Clock 32.768KHz



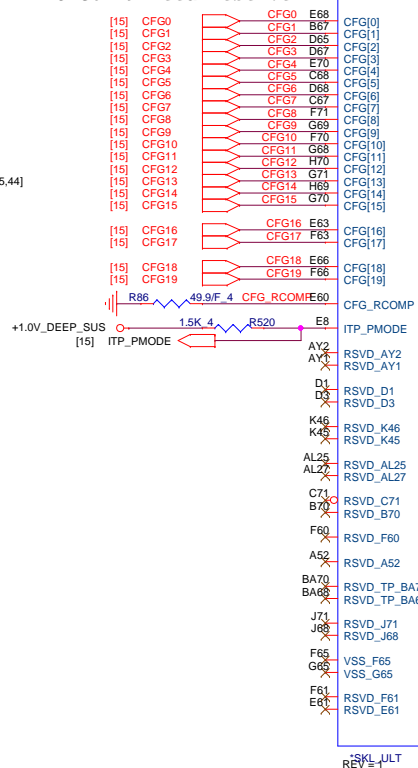
CLK_REQ/Strap Pin(CLG) +3V



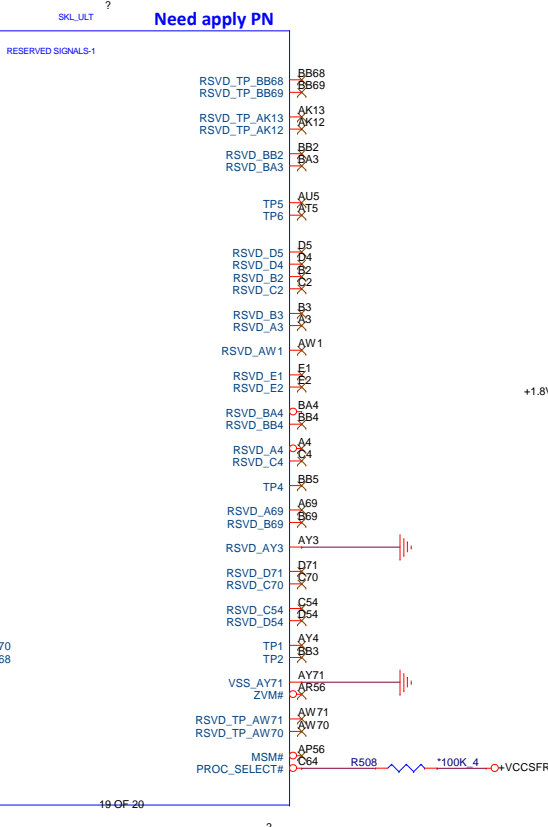
RTC Circuitry(RTC)



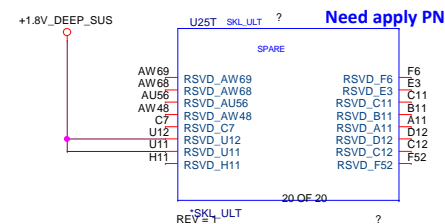
CFG0-19 need Reserve TP



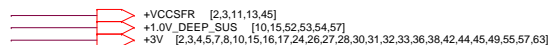
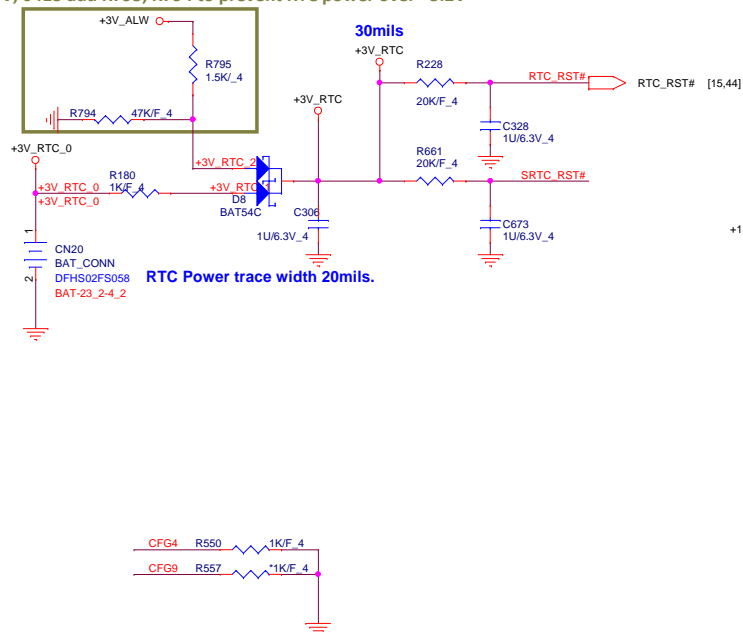
Need apply PN

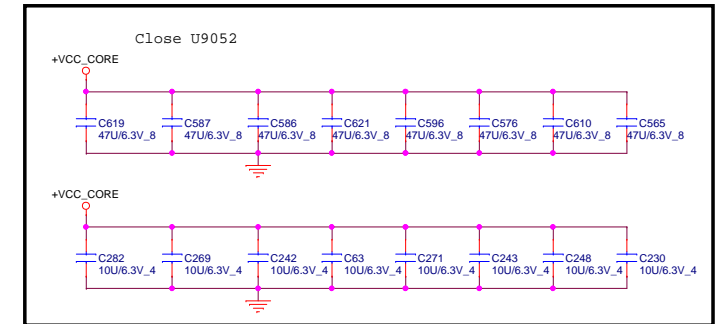
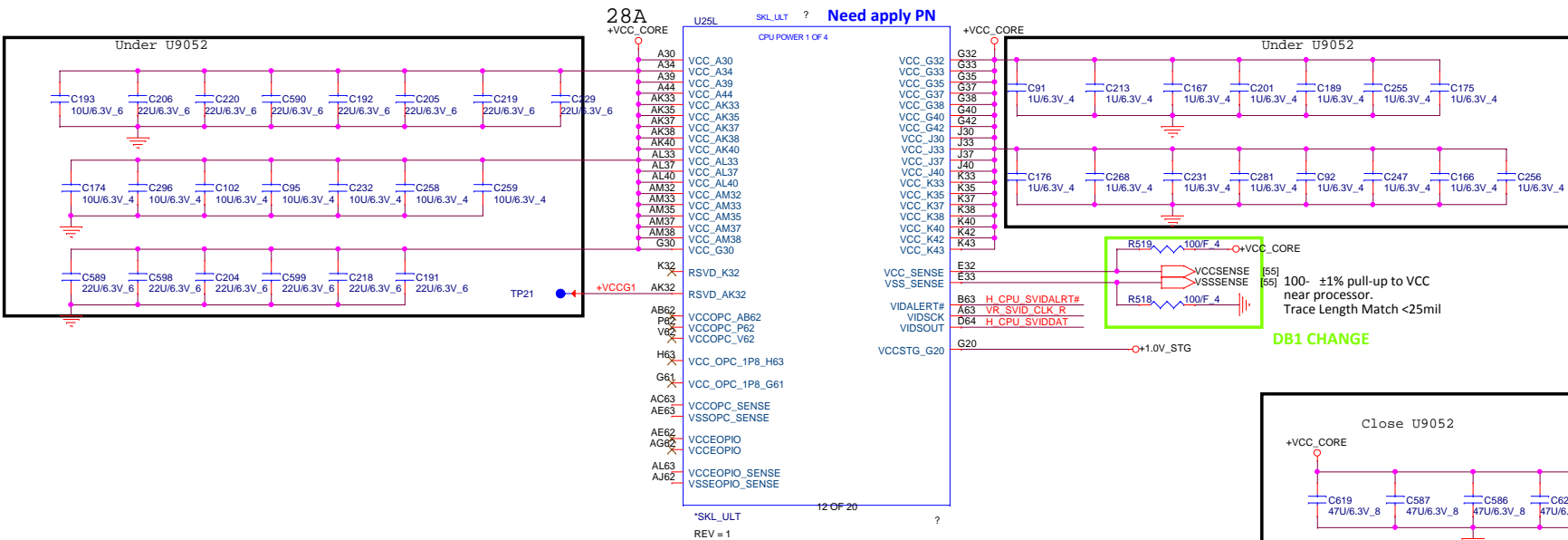


Need apply PN

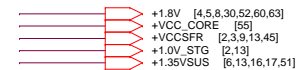
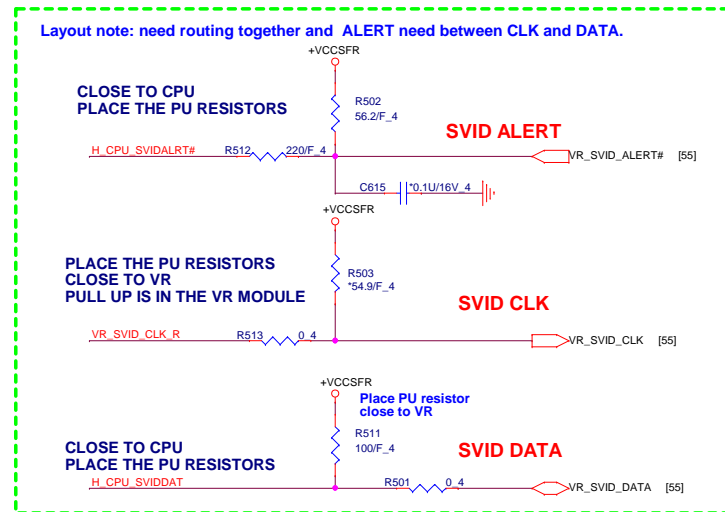


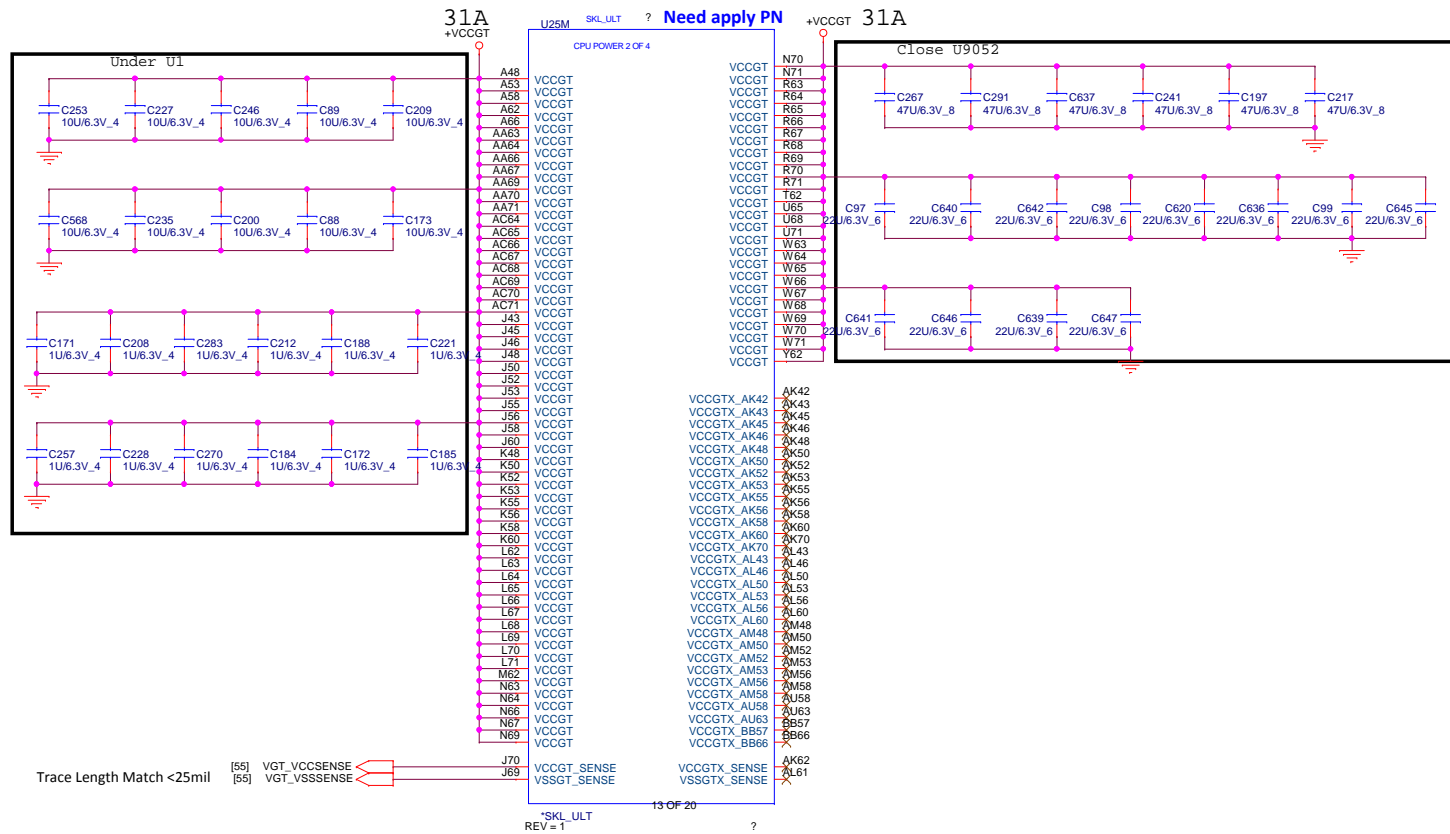
PV, 0413 add R795, R794 to prevent RTC power over +3.2V






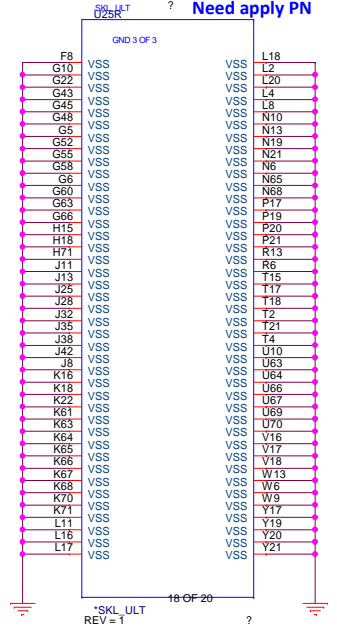
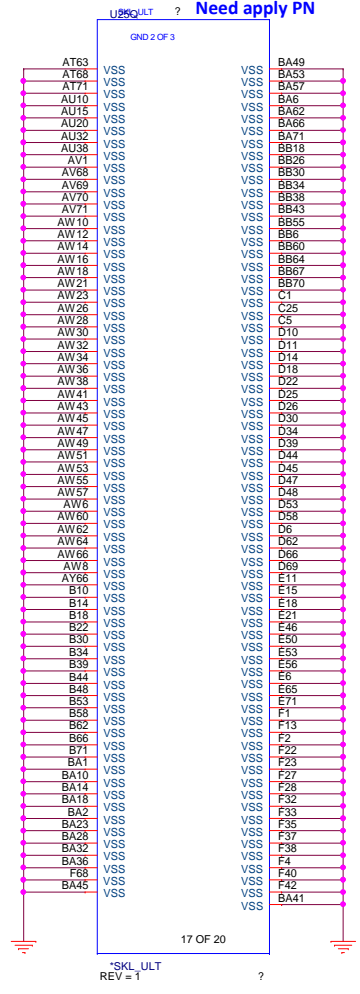
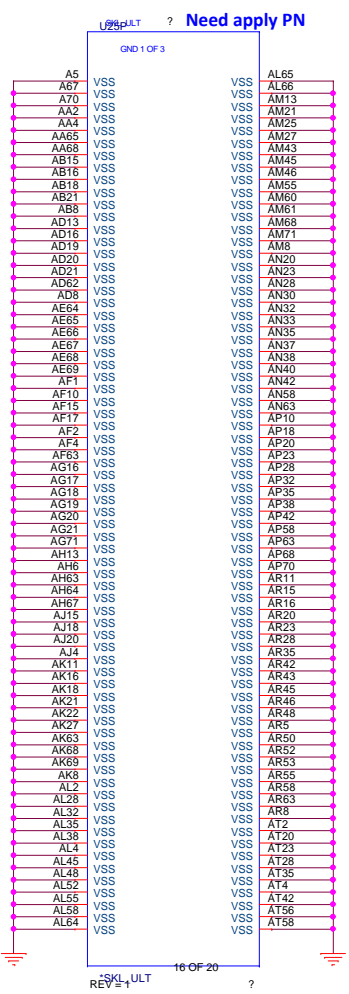
| Power Rail | Description | Control |
|------------------------|---|--|
| V _{CC} | Processor IA Cores Power Rail | SVID |
| V _{CCGT} | Processor Graphics Power Rails | SVID |
| V _{CCGTx} | Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs | SVID |
| V _{CCSA} | System Agent Power Rail | SVID/Fixed (SKU dependent) |
| V _{CCIO} | IO Power Rail | Fixed |
| V _{CCST} | Sustain Power Rail | Fixed |
| V _{CCPLL} | Processor PLLs power rail | Fixed |
| V _{DDQ} | Integrated Memory Controller Power Rail | Fixed (Memory technology dependent) |
| V _{CCOPC} | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| V _{CCOPC_1P8} | Processor OPC power rail (available only in SKU's with OPC) | Fixed |
| V _{CCEOPIO} | Processor EOPIO power rail (available only in SKU's with OPC) | Fixed |



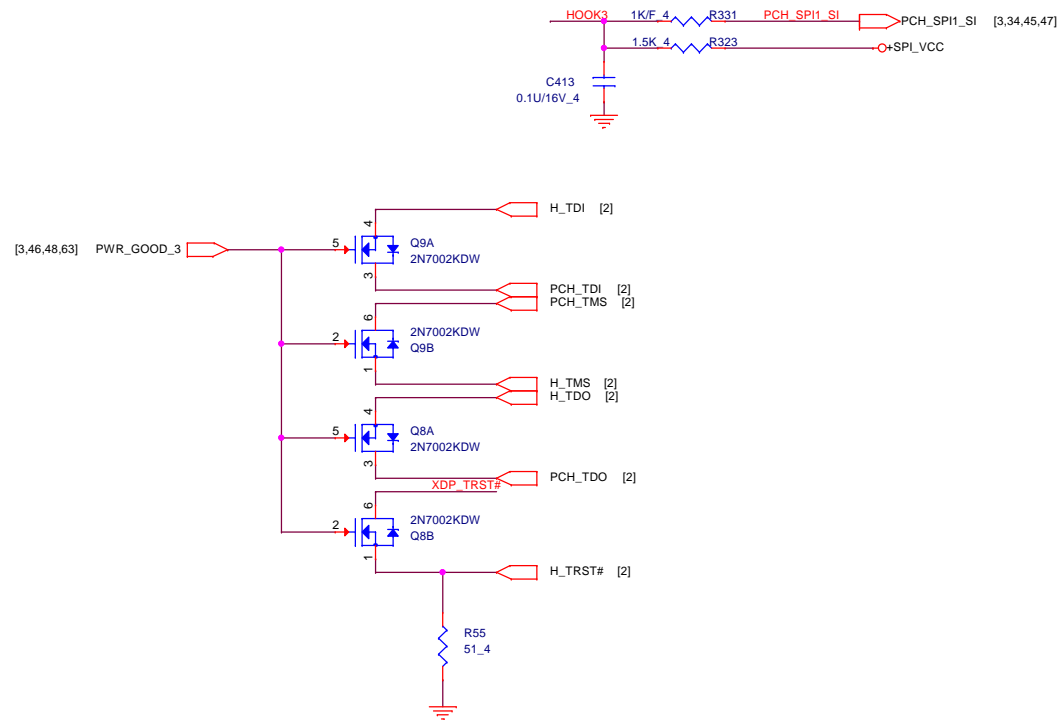
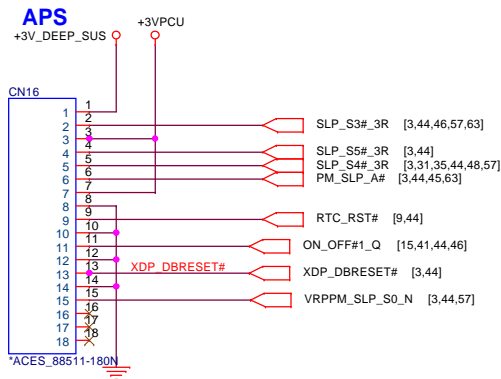
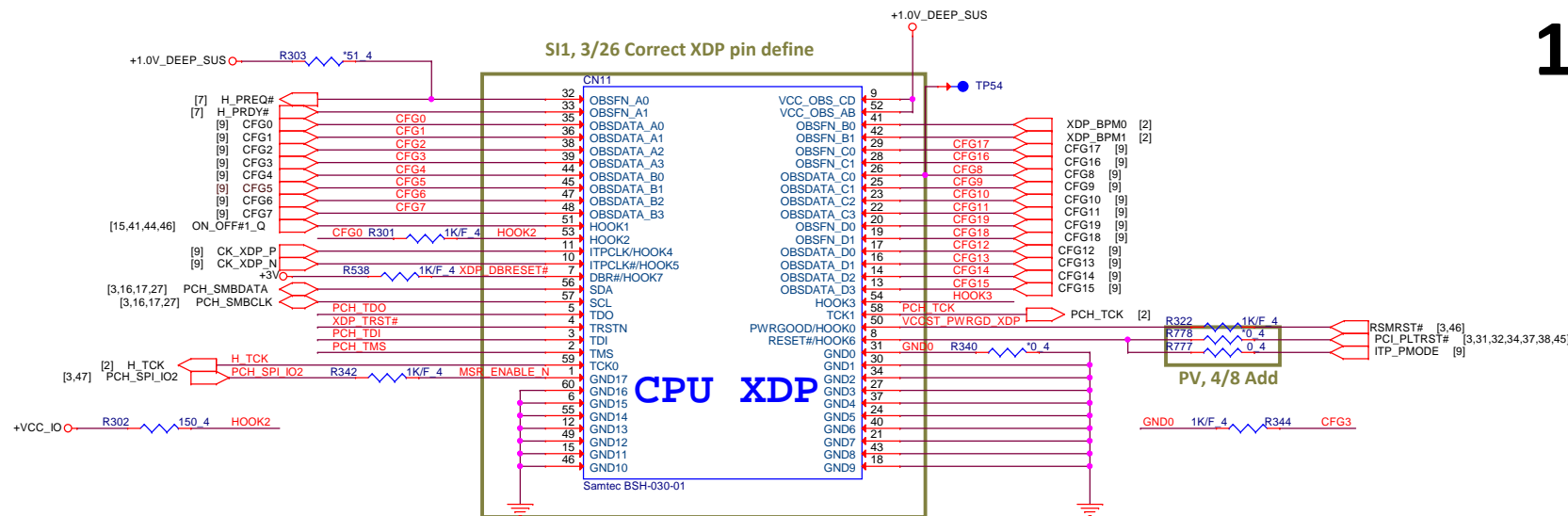




| | | | | |
|--|--|---|----|-----------|
|  NB5 | PROJECT:400 Series Quanta Computer Inc. | | | |
| | Size Custom | Document Number 13 -- SKYLAKE (POWER-3) | | Rev 1A |
| Date: Friday, April 17, 2015 | Sheet | 13 of | 25 | |



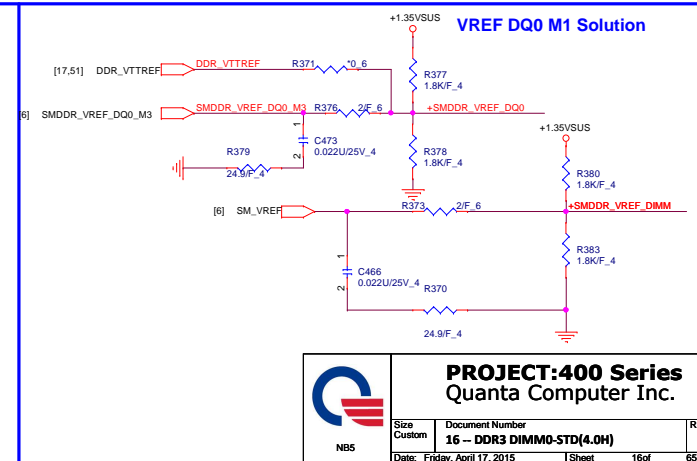
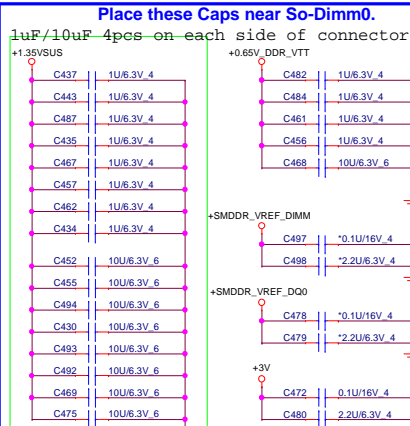
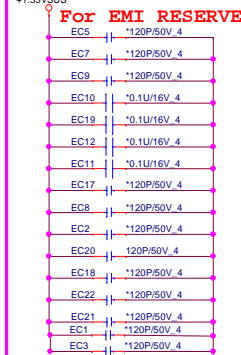
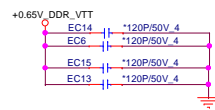
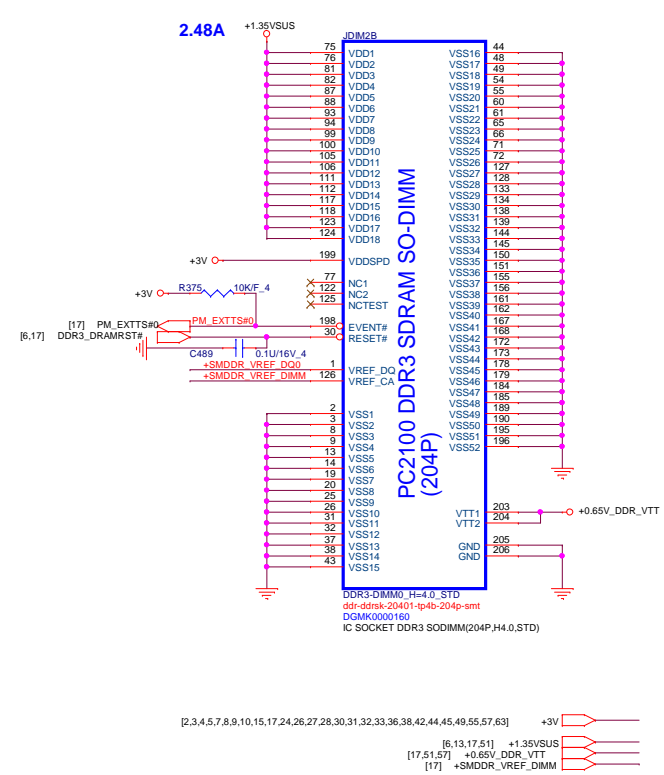
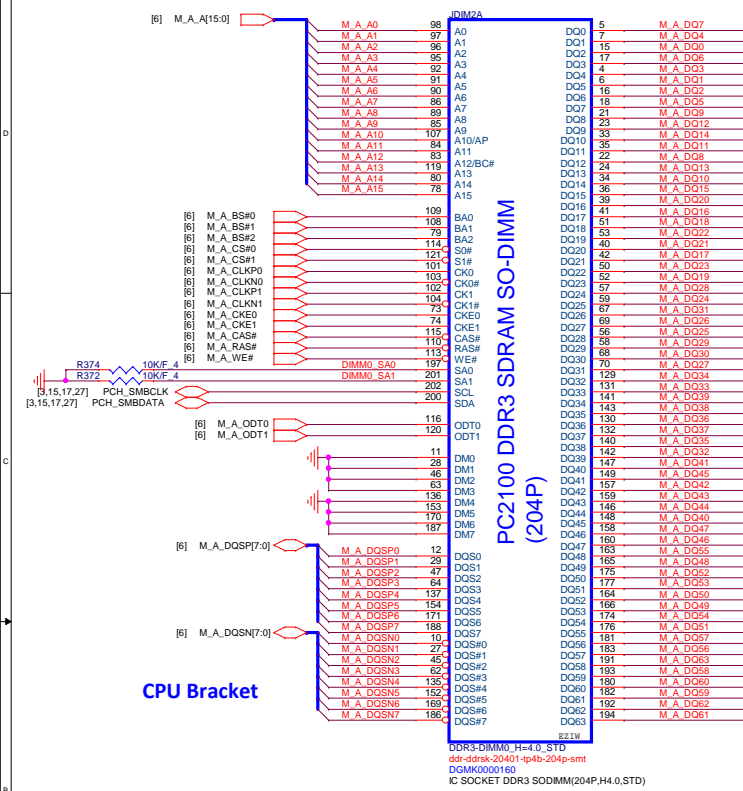
SI1, 3/26 Correct XDP pin define

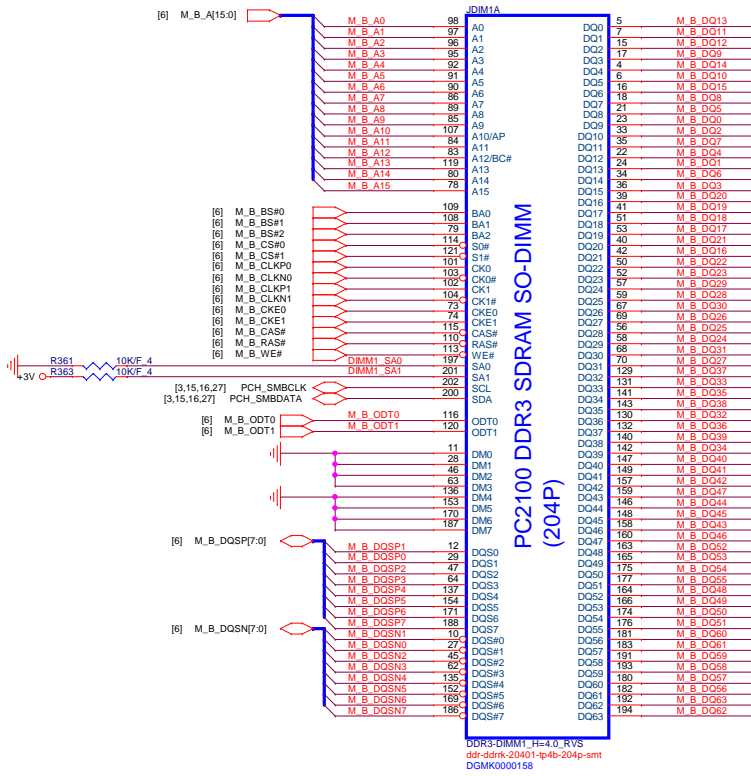


PROJECT:400 Series
Quanta Computer Inc.

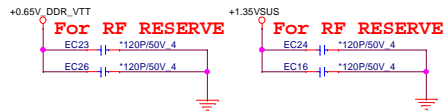
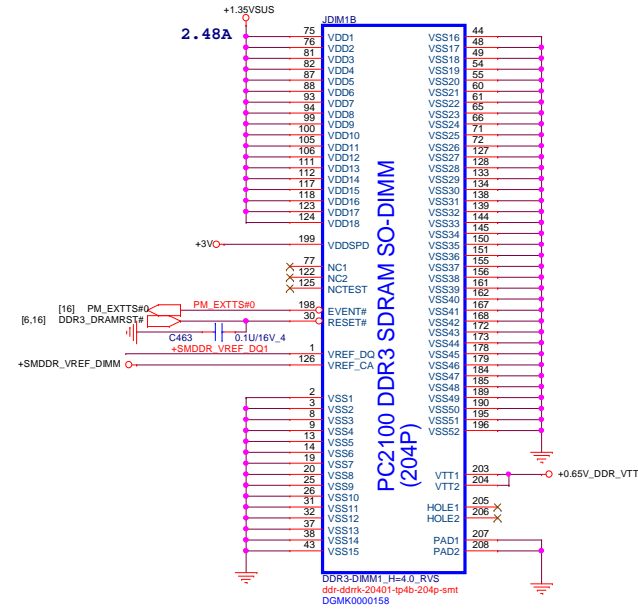
| | | |
|------------------------------|--------------------------------|-----|
| Size | Document Number | Rev |
| | 15 -- HSW XDP & APS | 1A |
| Date: Friday, April 17, 2015 | Sheet 15 of 65 | |

DIMM & Footprint 同Joshua提供





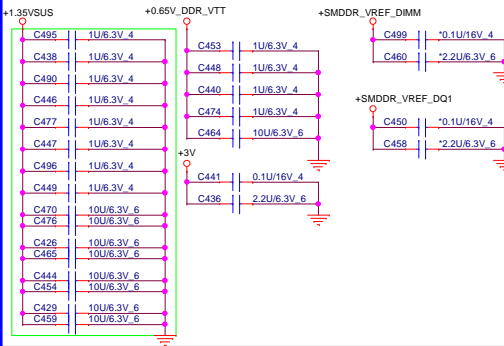
M_B_DQ[63:0] [6]



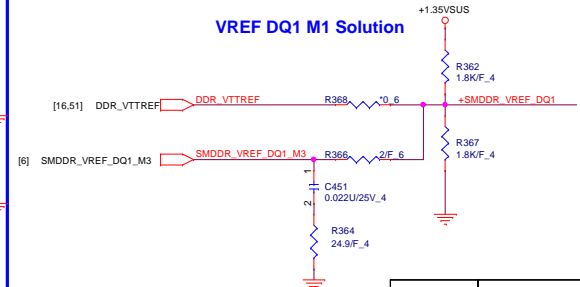
[6,13,16,51] +1.35VSUS
[16,51,57] +0.65V_DDR_VTT
[2,3,4,5,7,8,9,10,15,16,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V

Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution

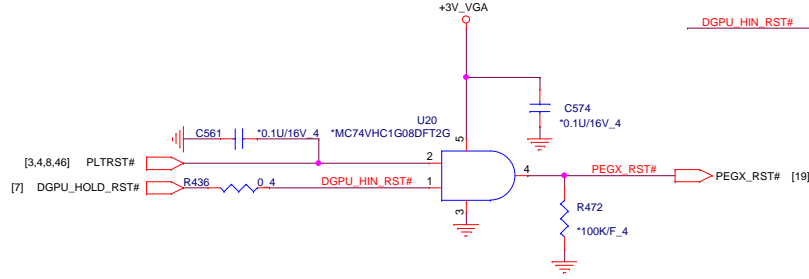
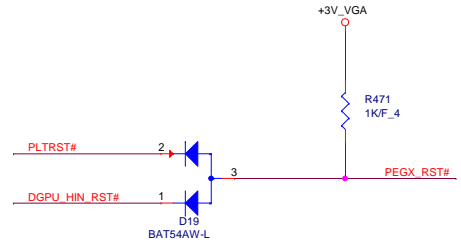
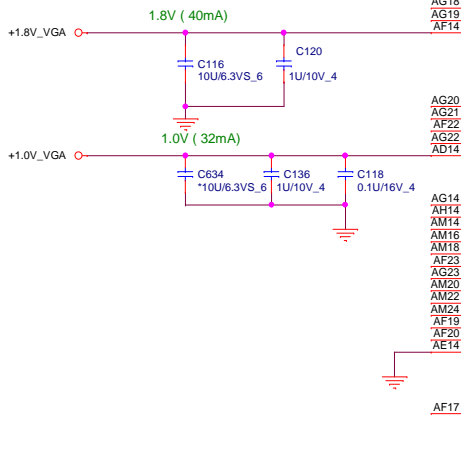
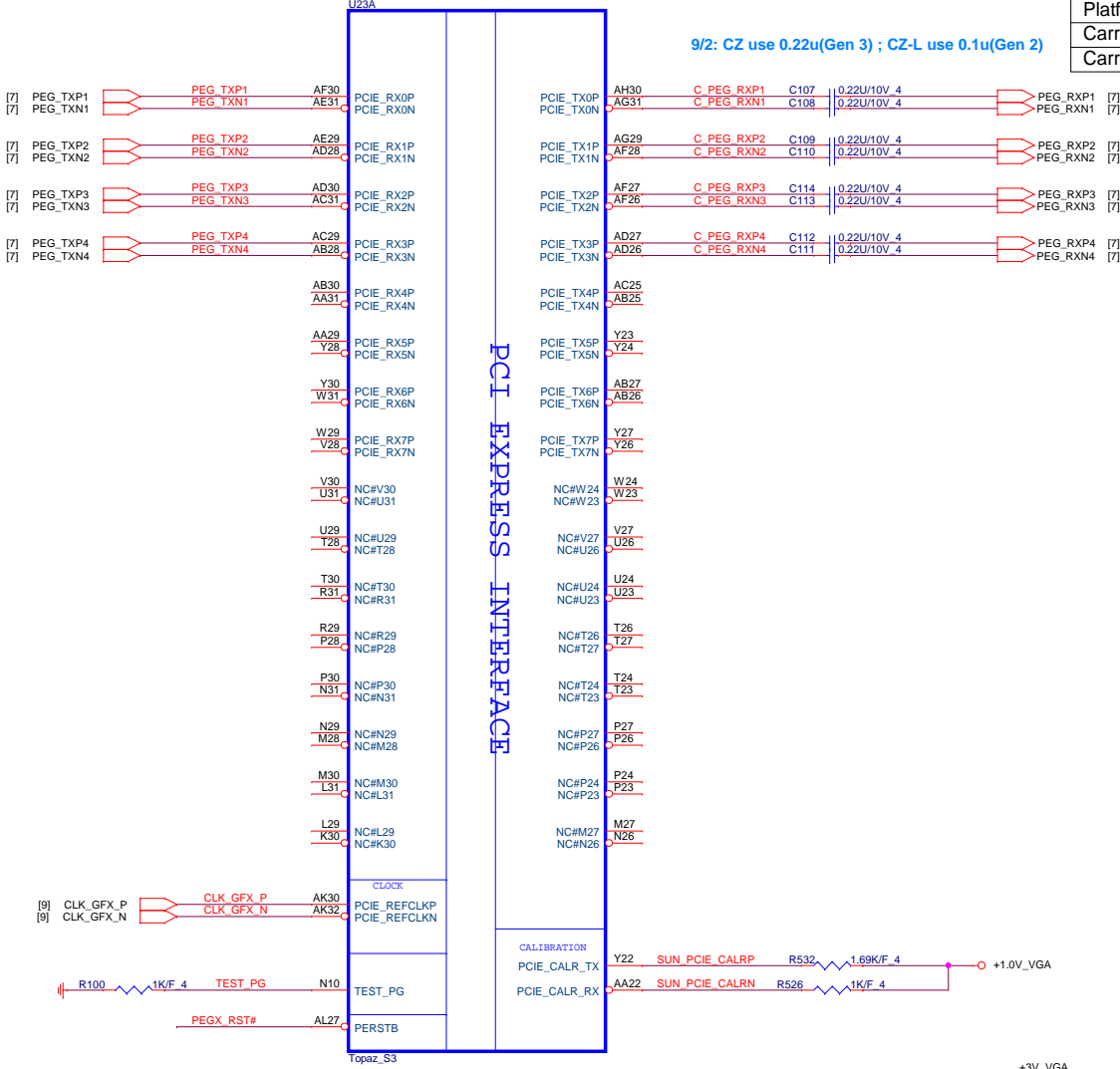



PROJECT:400 Series
Quanta Computer Inc.

| Size | Document Number | Rev |
|------------------------------|---------------------------|----------|
| Custom | 17 - DDR3 DIMM1-RVS(4.0H) | 1A |
| Date: Friday, April 17, 2015 | Sheet | 17 of 65 |

| Platform | Type | P/N |
|-----------|-------------|-------------|
| Carrizo | Gen 3 | CH4222K9B04 |
| Carrizo-L | Gen 1/Gen 2 | CH4102K1B03 |

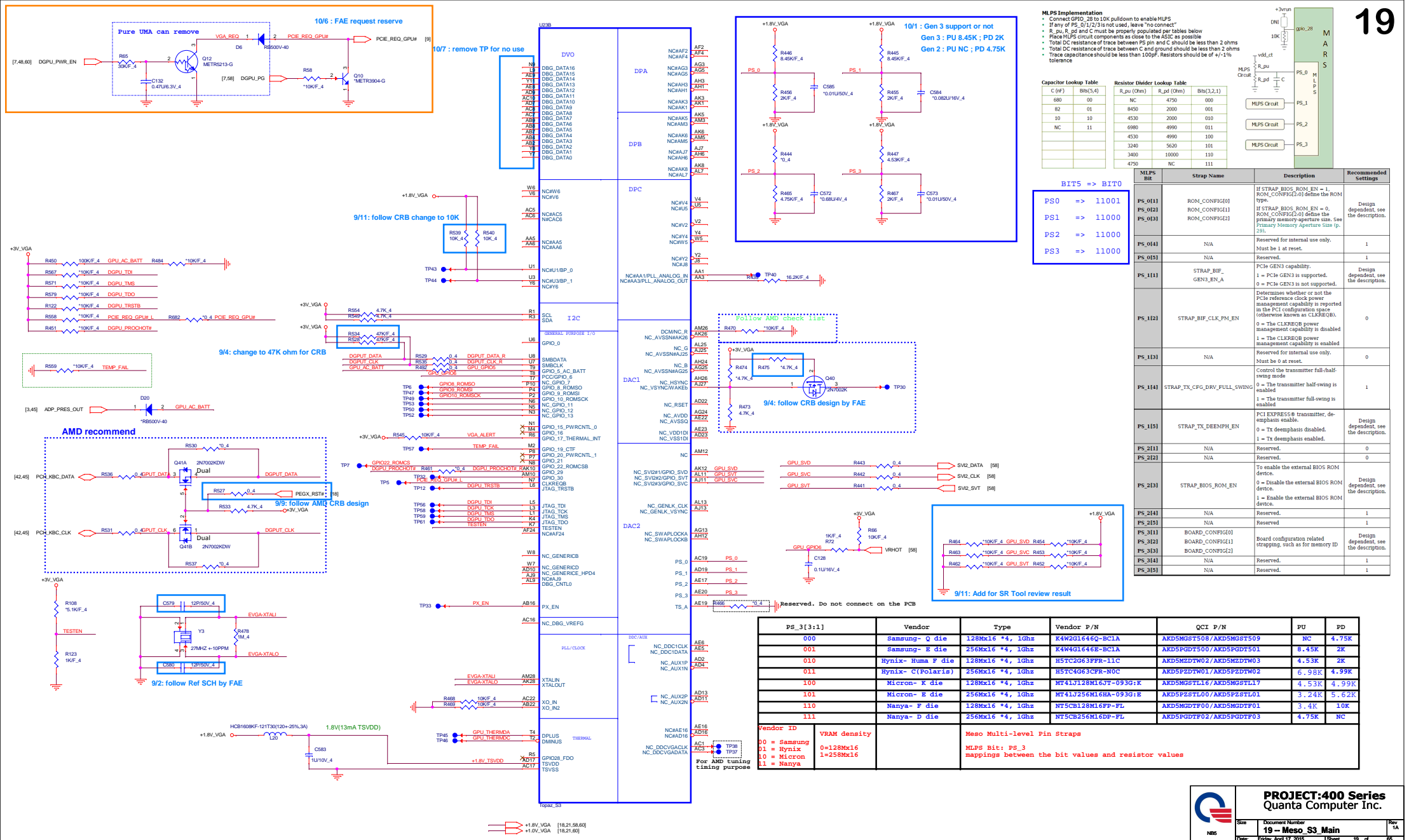
9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)

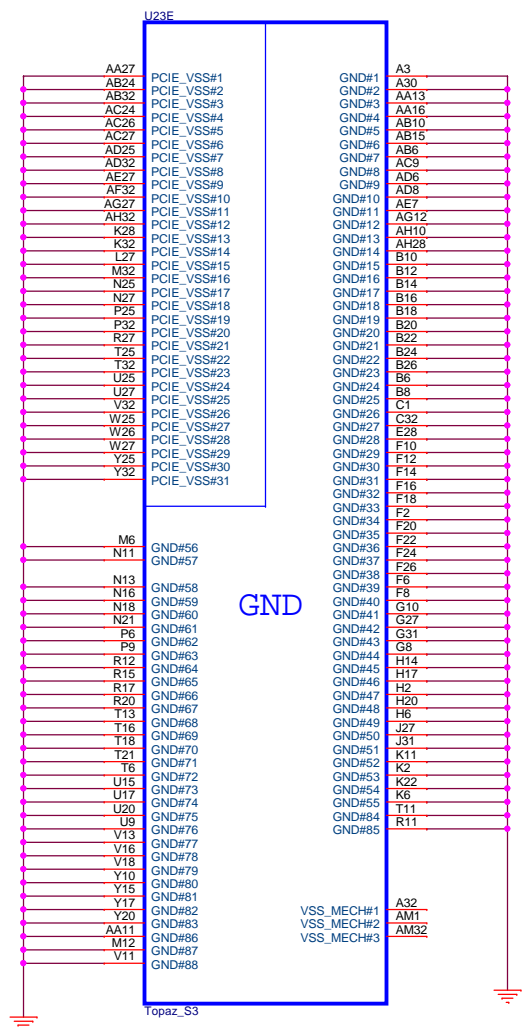




PROJECT:400 Series
Quanta Computer Inc.

| | | |
|-------|------------------------------------|----------------|
| Size | Document Number | Rev |
| NB5 | 18 -- Meso_S3_PCIE/DP POWER | 1A |
| Date: | Friday, April 17, 2015 | Sheet 18 of 65 |





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | |
|----------------------|----------------|---|--------|
| TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING | 0 |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED | X |
| RSVD | GPIO2 | RESERVED | 0 |
| RSVD | GPIO8 | RESERVED | 0 |
| BIF_VGA_DIS | GPIO9 | VGA ENABLED | 0 |
| RSVD | GPIO21 | RESERVED | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM | 0 |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | 0 0 1 |
| VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler) | 0 |
| RSVD | H2SYNC | RESERVED | 0 |
| AUD[1] AUD[0] | HSYNC VSYNC | SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL | 0 0 |
| RSVD | GENERICC | RESERVED | 0 |

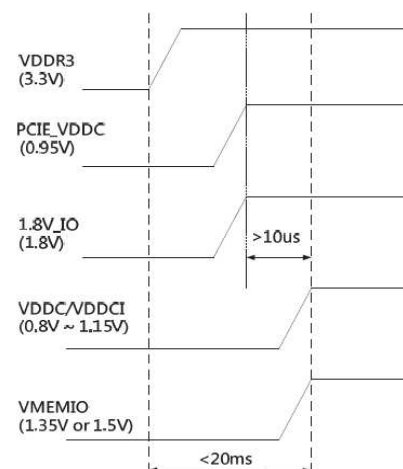
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

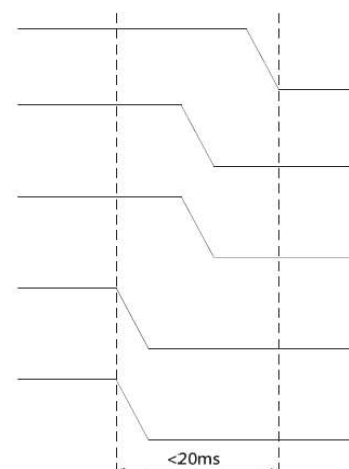
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

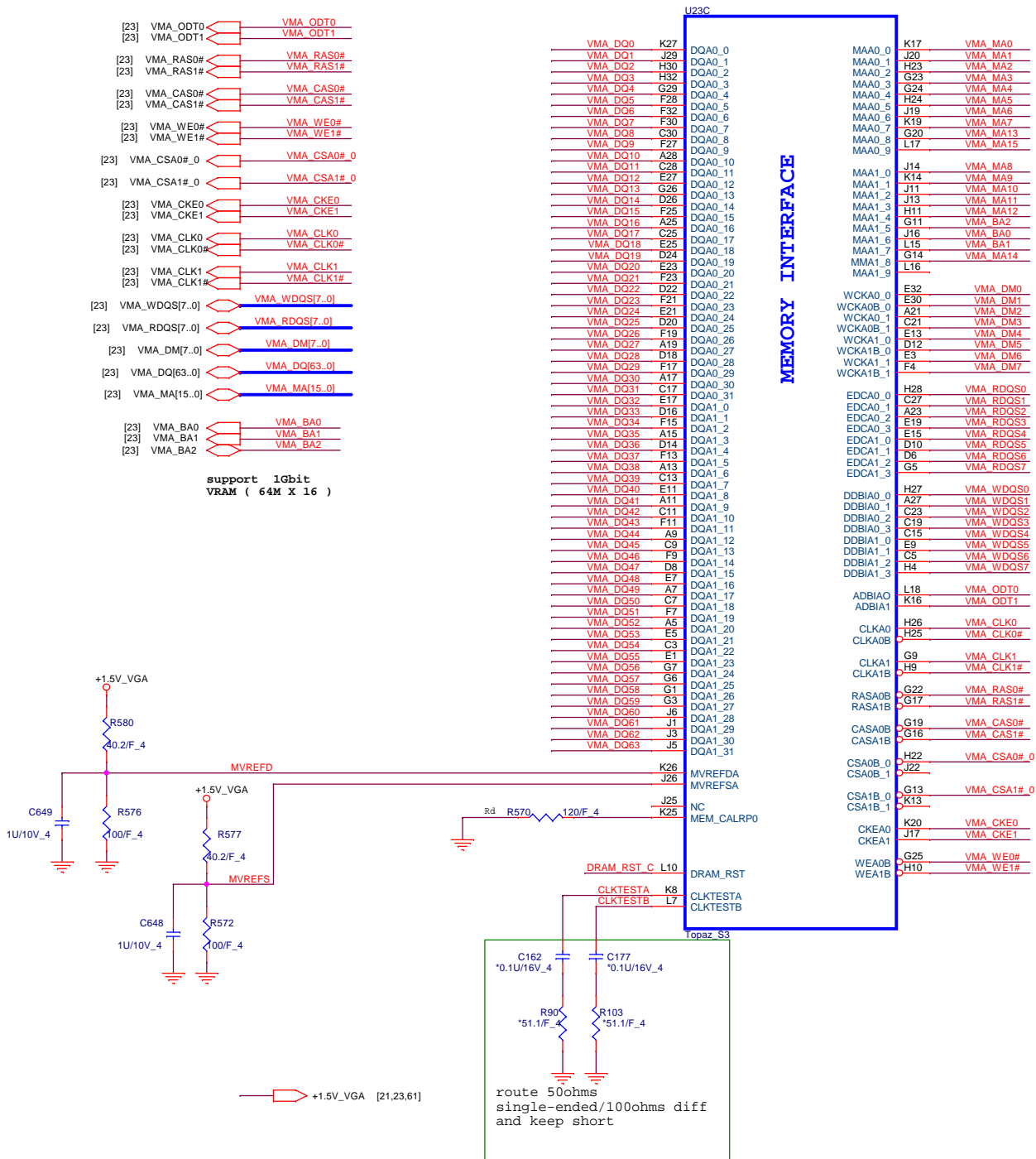


POWER DOWN



PROJECT:400 Series
Quanta Computer Inc.

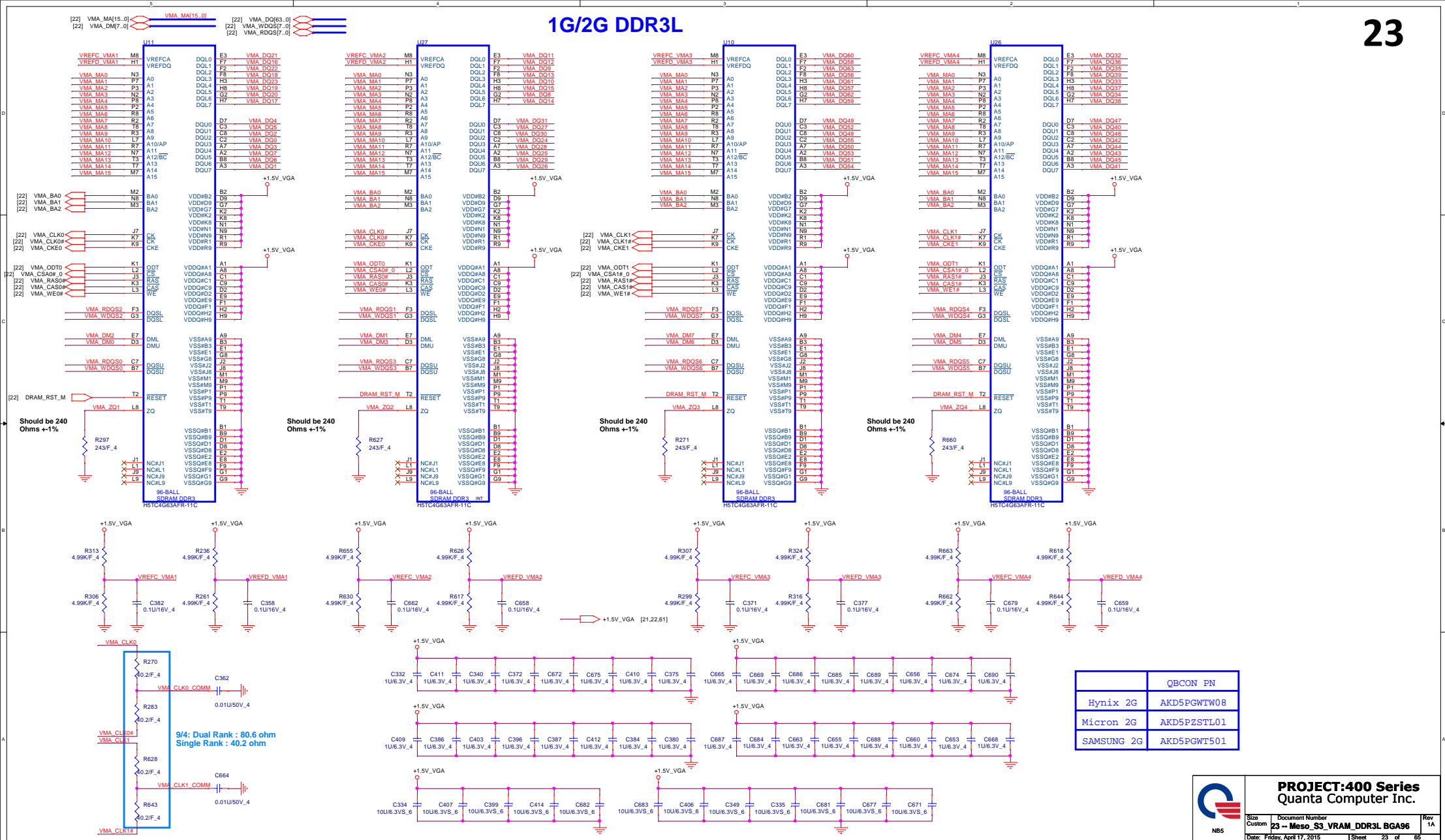
| | | |
|-------|------------------------------------|----------------|
| Size | Document Number | Rev |
| | 20 - Meso_S3_GND/LVDS/Strap | 1A |
| Date: | Friday, April 17, 2015 | Sheet 20 of 65 |



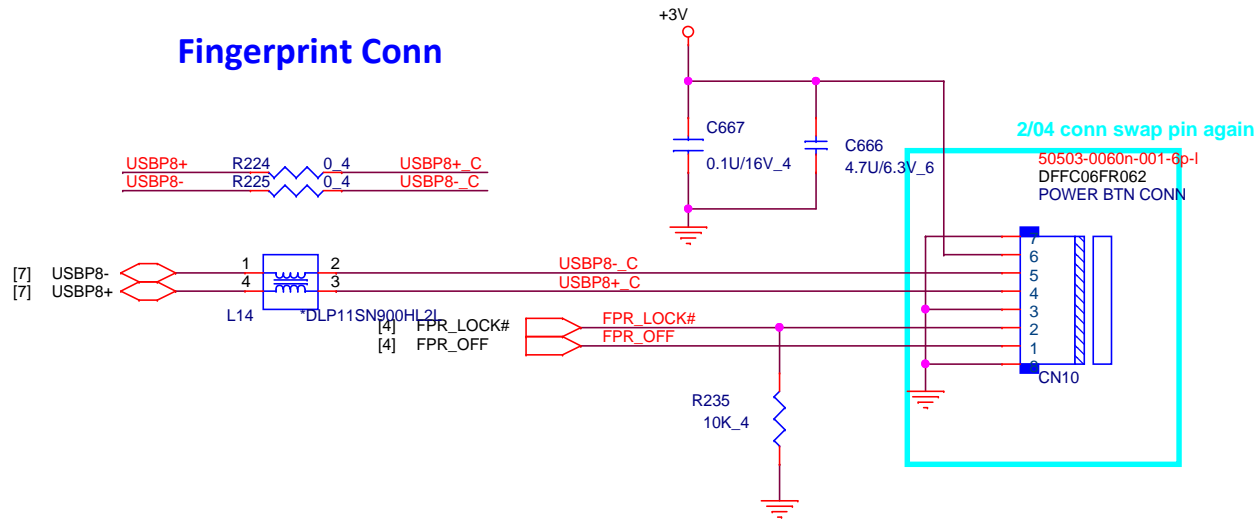
PROJECT:400 Series Quanta Computer Inc.

| Size | Document Number | Rev |
|------------------------------|-----------------------|----------|
| 22 | Meso_S3_MEM_Interface | 1A |
| Date: Friday, April 17, 2015 | Sheet | 22 of 65 |

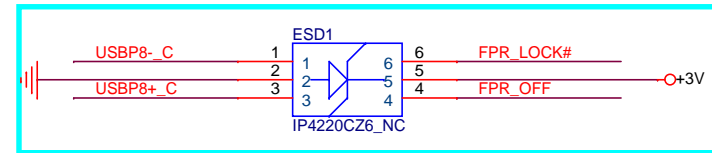
1G/2G DDR3L



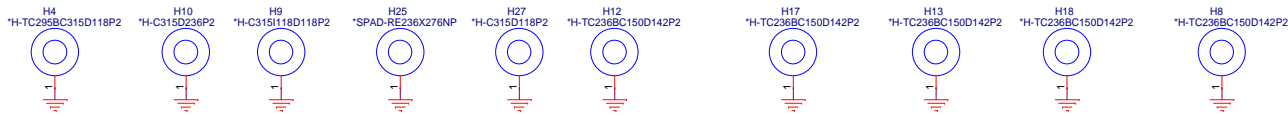
Fingerprint Conn



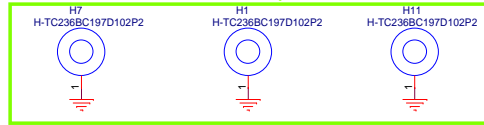
2/11 ESD1 swap pin



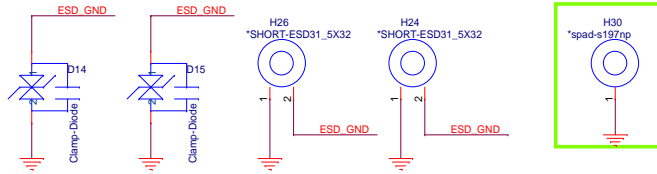
Hole



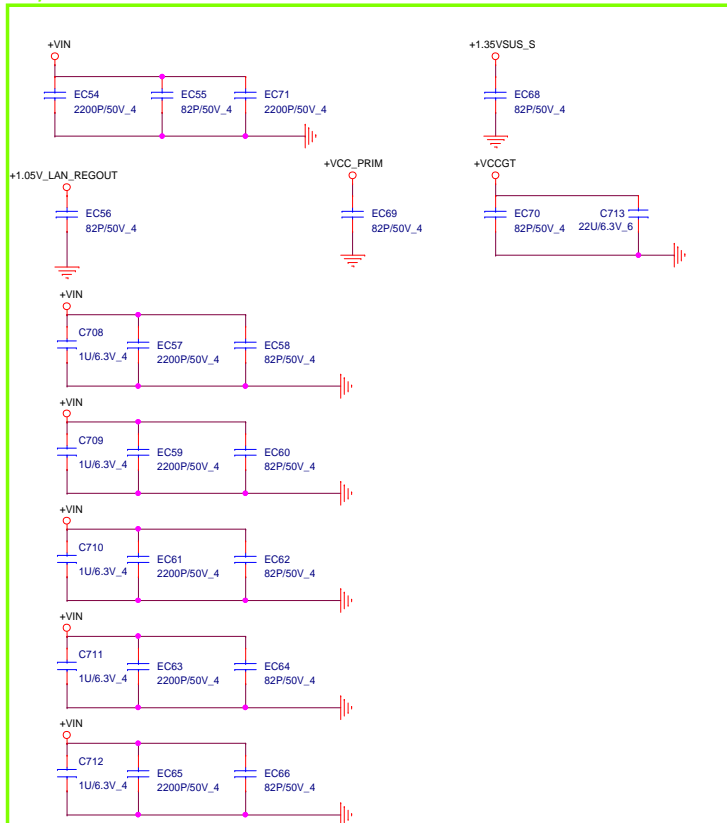
02/03 DB1 to SI



02/11 DB1 to SI

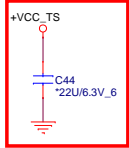
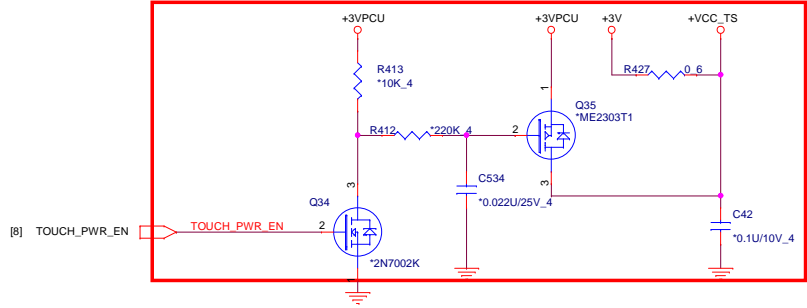
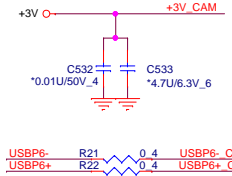
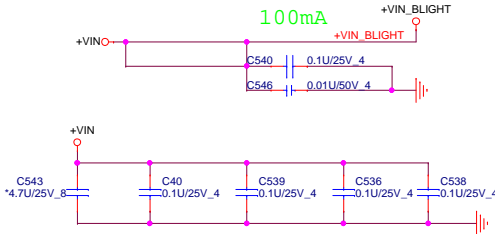
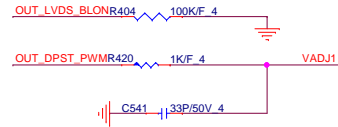
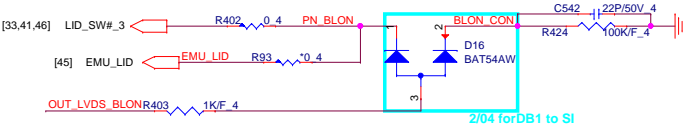


02/04 DB1 to SI for RF

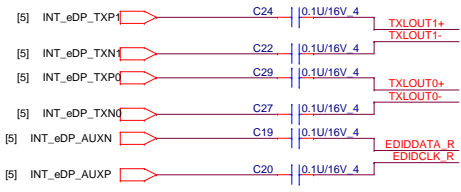
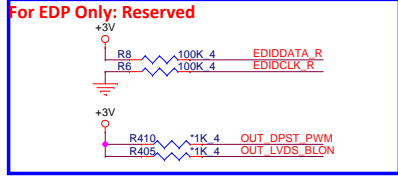
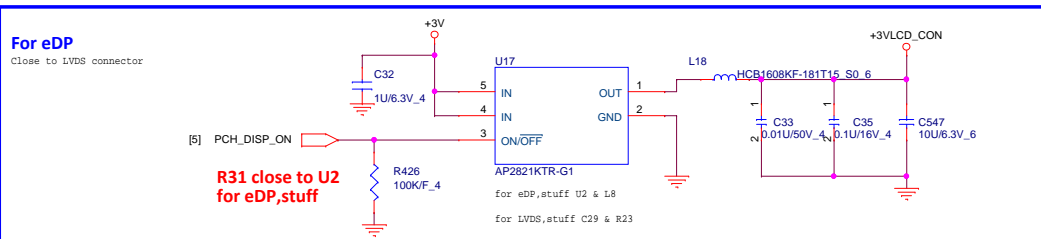
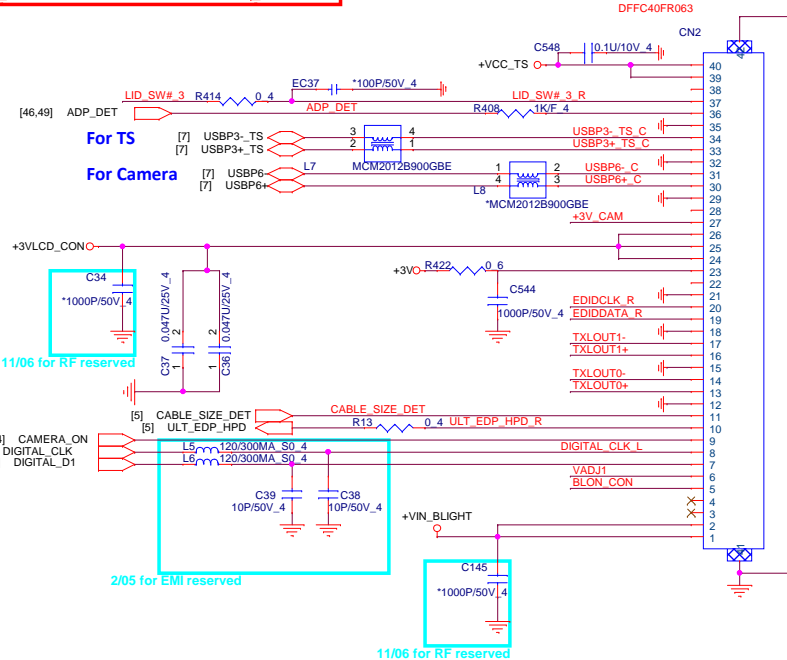


LID Switch

LVDS Conn. 26



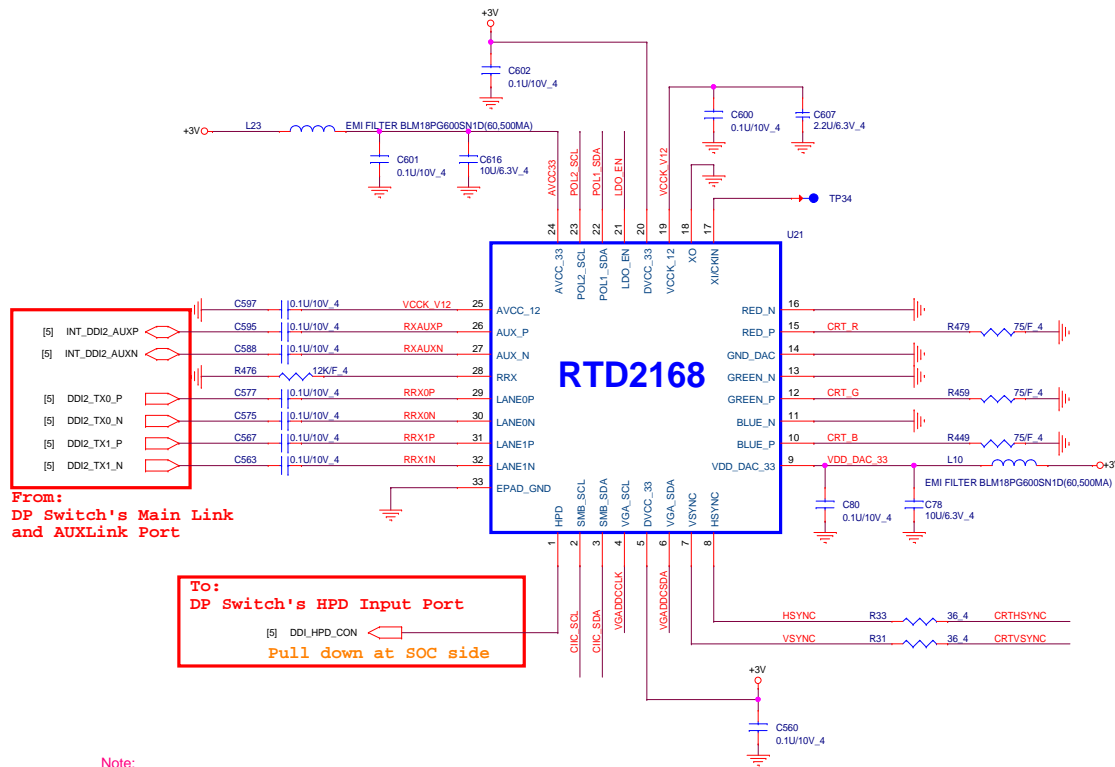
GS12401-1011-9H
lvs-50671-04041-001-40p-I



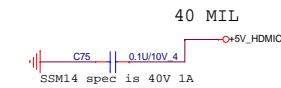
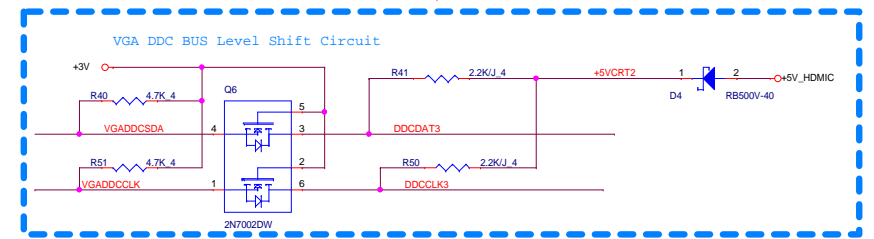
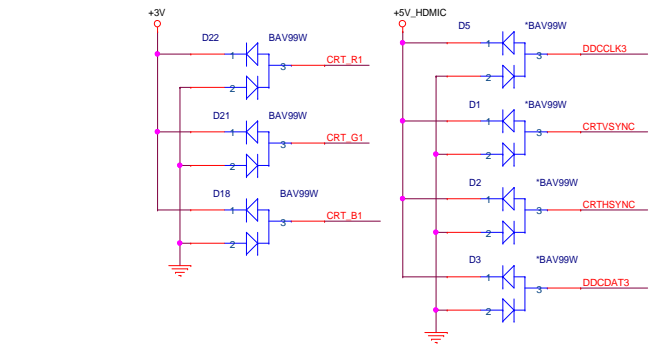
[2,3,4,5,7,8,9,10,15,16,17,24,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V

[8,29,30,31,40,42,43,52,57,63] +5V

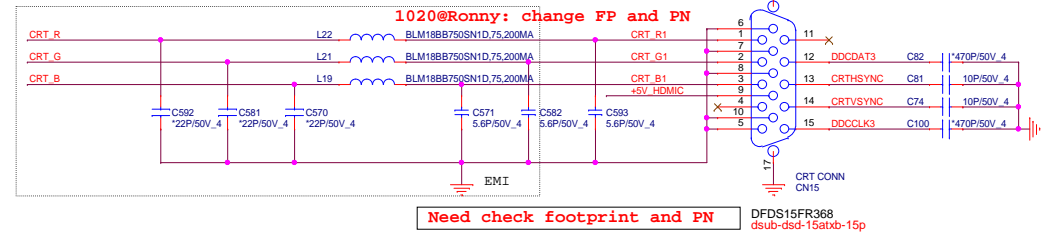
[25,44,49,50,51,52,53,54,55,56,57,59,61] +VIN



- Note:
- 1- C1,C3,C6,C8,C9,C11,C12,C19,C20 Should be close to chip
 - 2- C12 should be X5R material
 - 3- R1 should be 12K ohm with +/-1%
 - 4- R8, R9, R10 should be 75 ohm with +/-1%

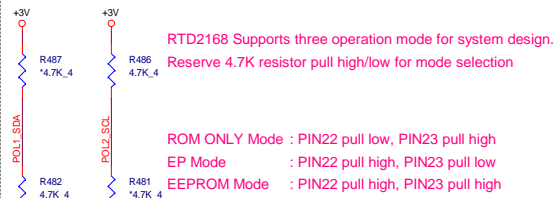


1103@RNY:
need change L11~L13 to 0402 size PN and value



Mode Configure Table(Power On Latch)

| | | POL1_SDA(PIN22) | |
|-----------------|---|-----------------|-------------|
| | | 0 | 1 |
| POL2_SCL(PIN23) | 0 | X | EP MODE |
| | 1 | ROM ONLY MODE | EPPROM MODE |



EEPROM MODE

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following conditions.

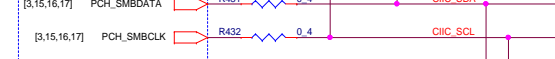
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

From PCH

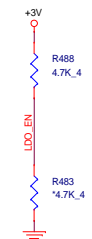


From EC



Embedded LDO

Select VCCK_V12 source from external 1.2V or embedded LDO

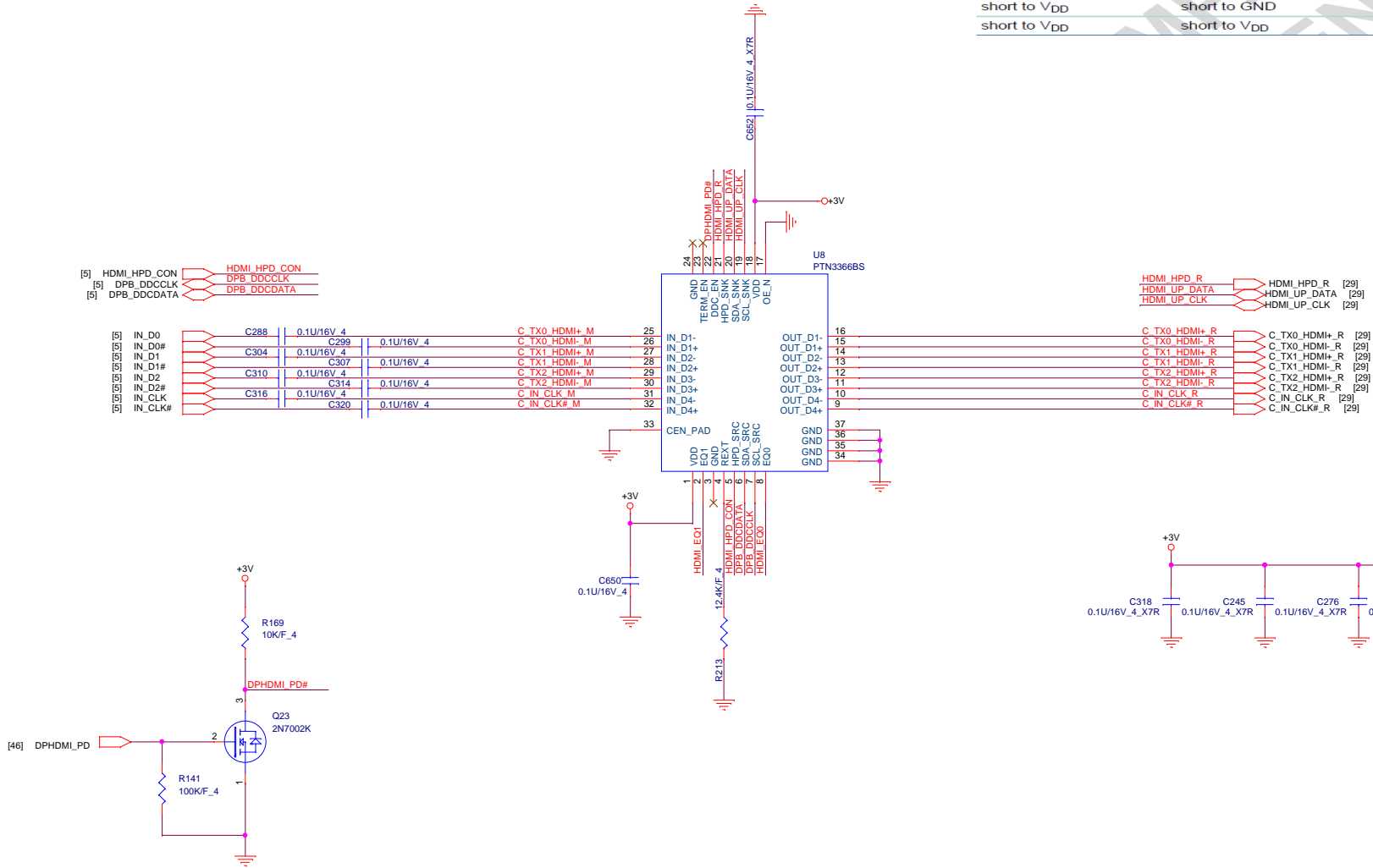



| LDO_EN(PIN21) | |
|-----------------------------|----------------------------|
| 0 | 1 |
| VCCK_V12 from External 1.2V | VCCK_V12 from Embedded LDO |



PROJECT : S Class-AMD
Quanta Computer Inc.

| Size | Document Number | Rev |
|------------------------------|-----------------|-----|
| Custom | DP to VGA | 1A |
| Date: Friday, April 17, 2015 | Sheet 27 of 65 | |



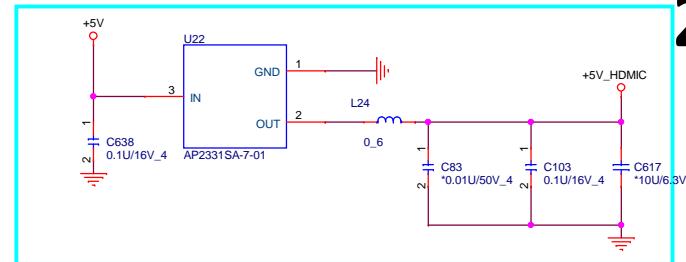
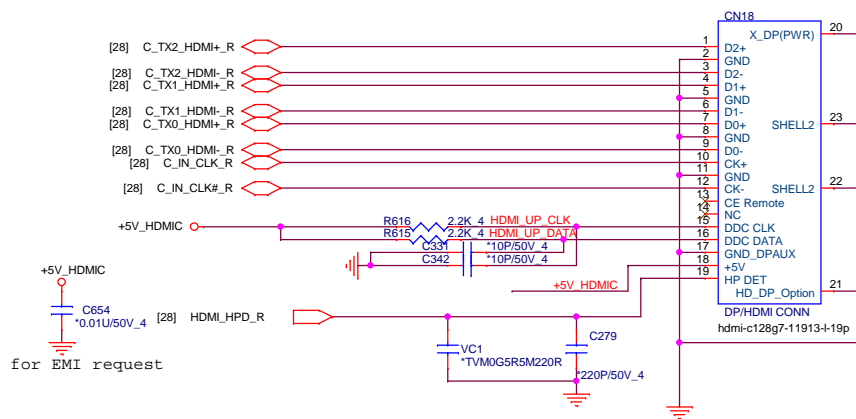
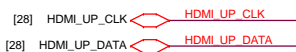
| | | | |
|--|--|---|-----------|
|  NB5 | PROJECT:400 Series Quanta Computer Inc. | | |
| | Size Custom | Document Number 28 – REPEATER PS8407A | Rev 1A |
| | Date: Friday, April 17, 2015 | Sheet 28 of 65 | |

11/06 for change new SW

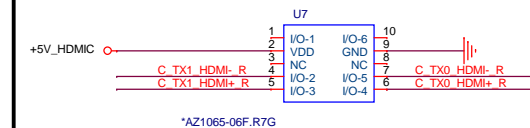
EMI Solution



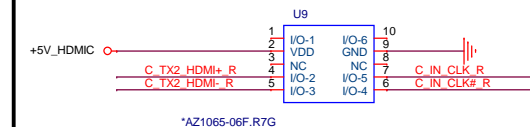
HDMI SMBus Isolation

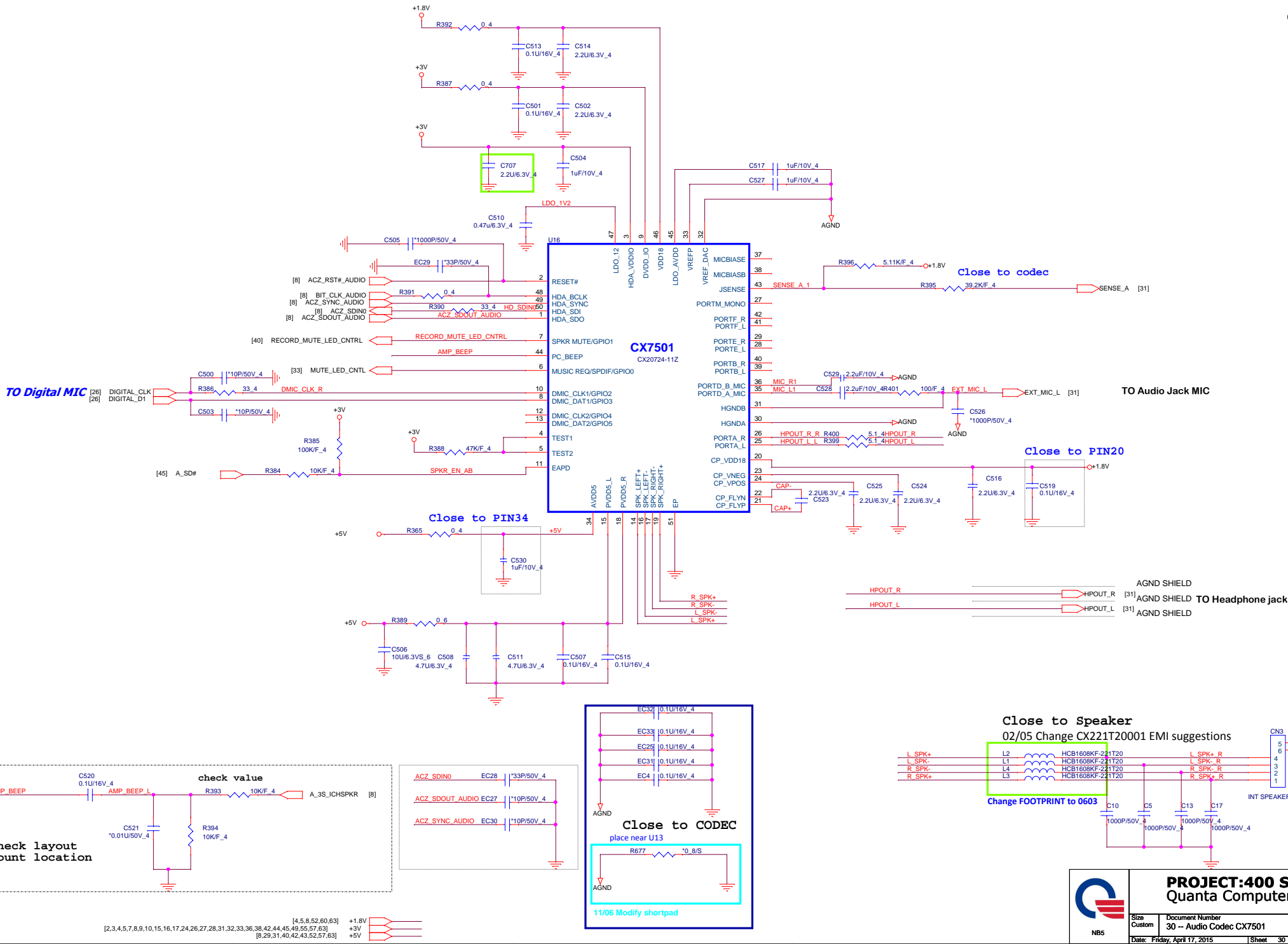


ESD chip, reserve

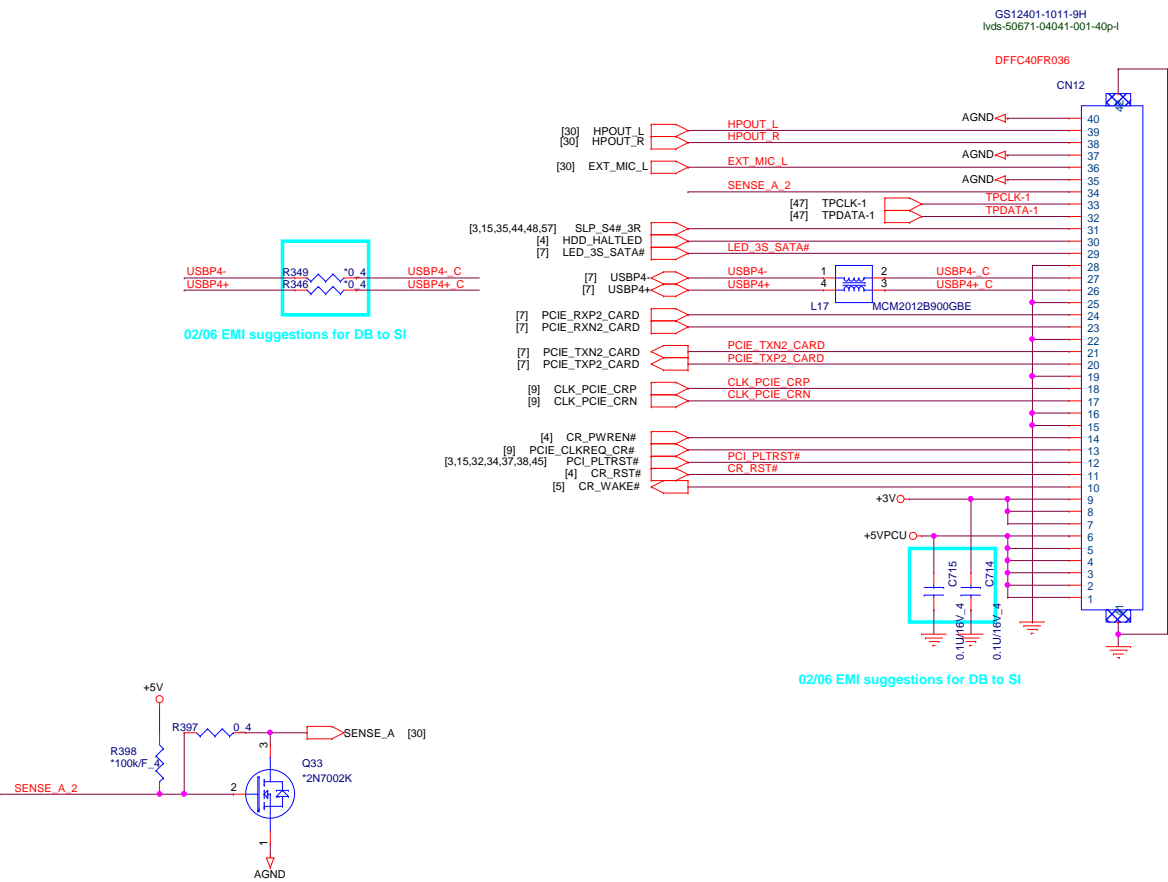


ESD chip, reserve





USB/Card Reader/Headphone_Mic Combo Jack Daugther Board Connector



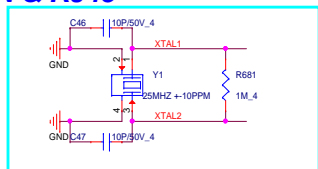
PROJECT:400 Series
Quanta Computer Inc.

| Size | Document Number | Rev |
|--------|----------------------------|-----|
| Custom | 31 -- DAUGHTER BOARD CONN. | 1A |

Date: Friday, April 17, 2015 Sheet 31 of 65

LAN & RJ45

04/13 for LAN reserved



Power trace Layout 寬度> 60mil

>60mil

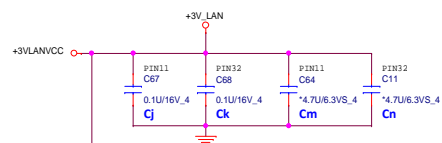
WIN_REGOUT

<30 mil

For SWR mode
 Stuff La, Ca ,Cb
 NA : Ra, Ci

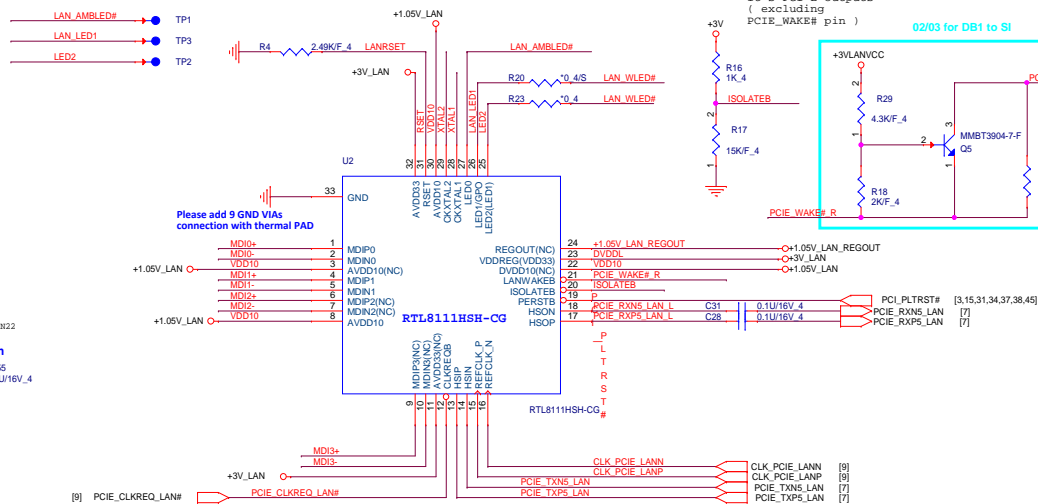
* Place Cj and Ck, close to each VDD33 pin-- 11, 32

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



For SWR mode
Stuff Co, Cp

Remove For Not Using SWR mode

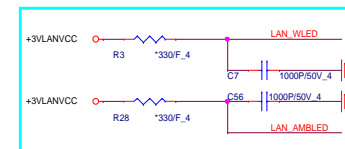


```
if ISOLATED pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

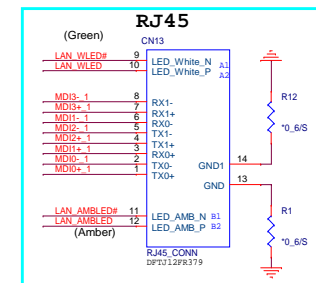
02/03 for DB1 to S

| | | |
|------------|---------------|-----------------------|
| 0.1U/16V_4 | PCI_PLTRST# | [3,15,31,34,37,38,45] |
| 0.1U/16V_4 | PCIE_RXN5_LAN | [7] |
| 0.1U/16V_4 | PCIE_RXP5_LAN | [7] |

02/13 for DB1 to SI



02/03 for DB1 to SI



For GiGA BOT:GST5009B LE DB0Z06LAN00

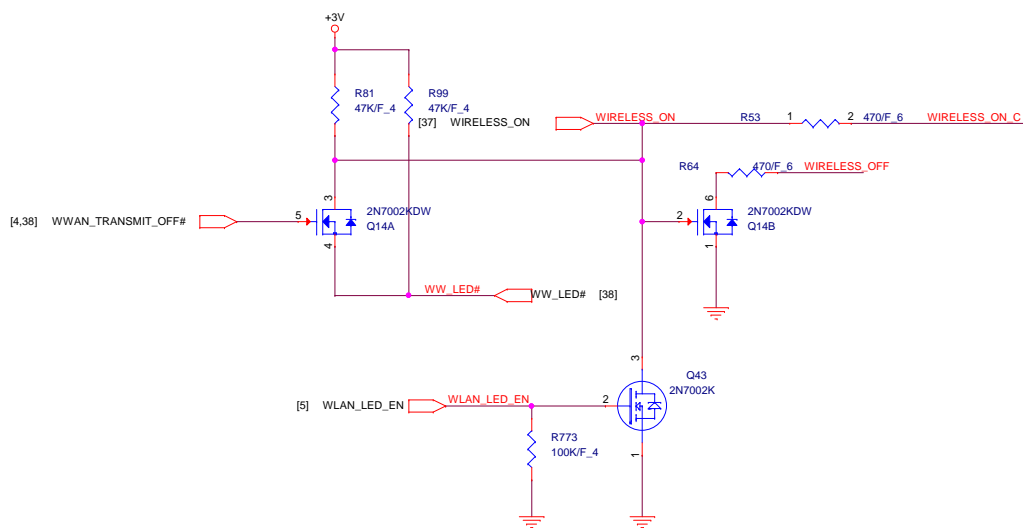
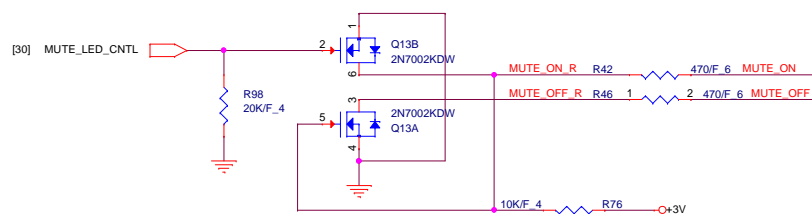
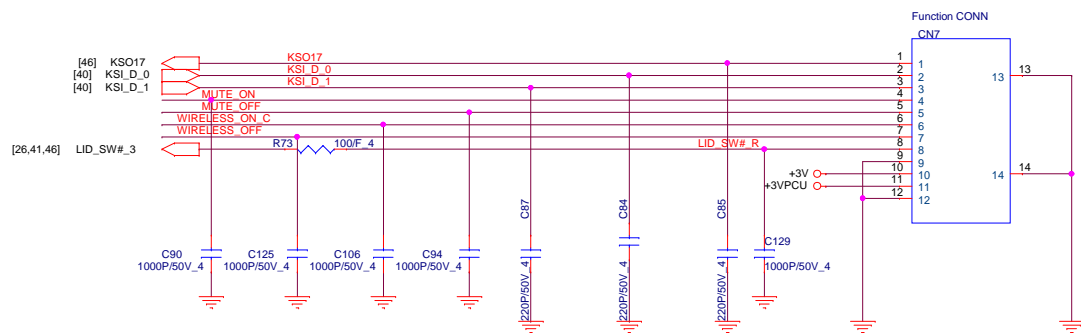
FCE :NS892407 ,DB0LL1LAN00

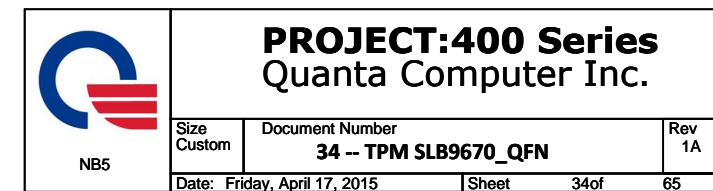
11/18 modify footprint

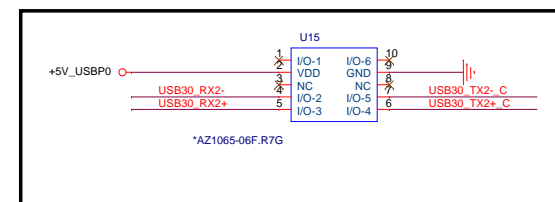
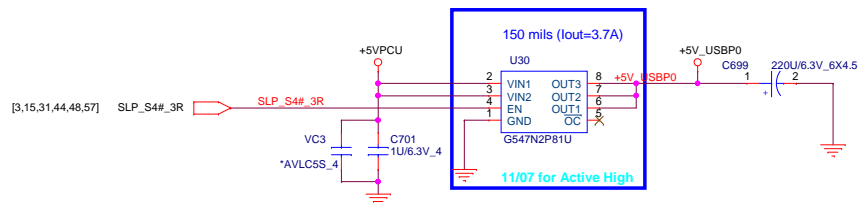
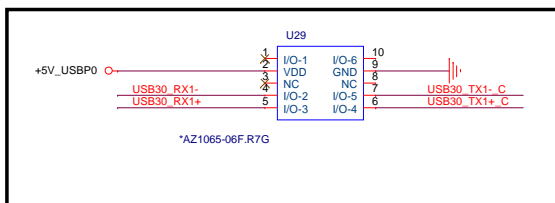
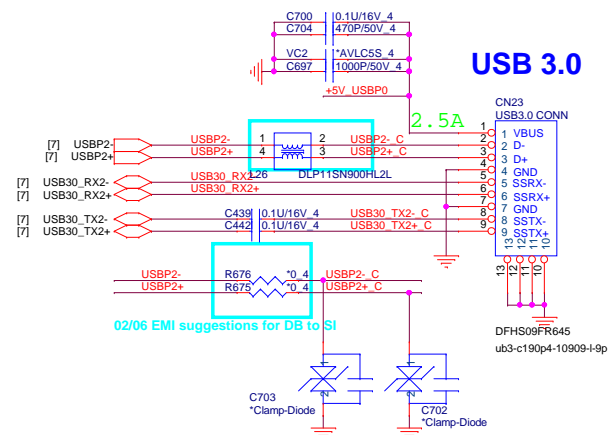
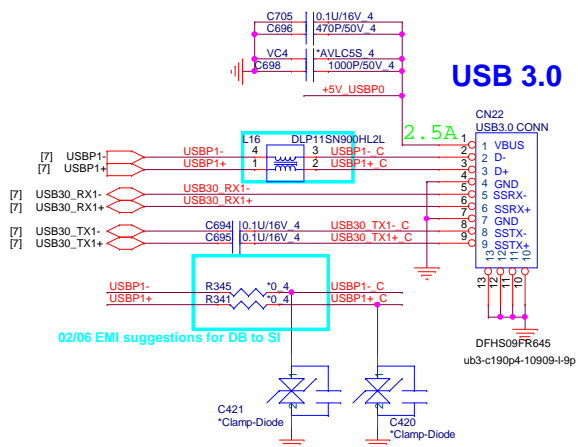
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,33,36,38,42,44,45,49,55,57,63]

+3V

[57] +3V
+3VLAVCC



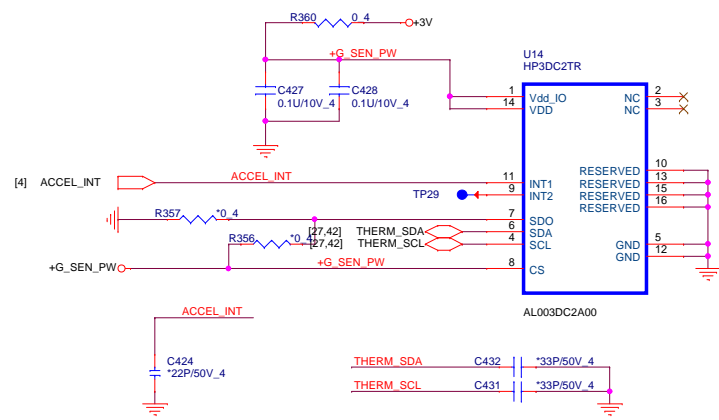




[31,49,50,51,52,55,56,57,58,60,61,63] +5VPCU


[3,10,15,26,33,37,38,40,41,42,44,45,46,49,50,53,54,57,60,62,63] +3VPCU

Accelerometer Sensor



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,38,42,44,45,49,55,57,63] +3V

[3,10,15,26,33,37,38,40,41,42,44,45,46,49,50,53,54,57,60,62,63] +3VPCU

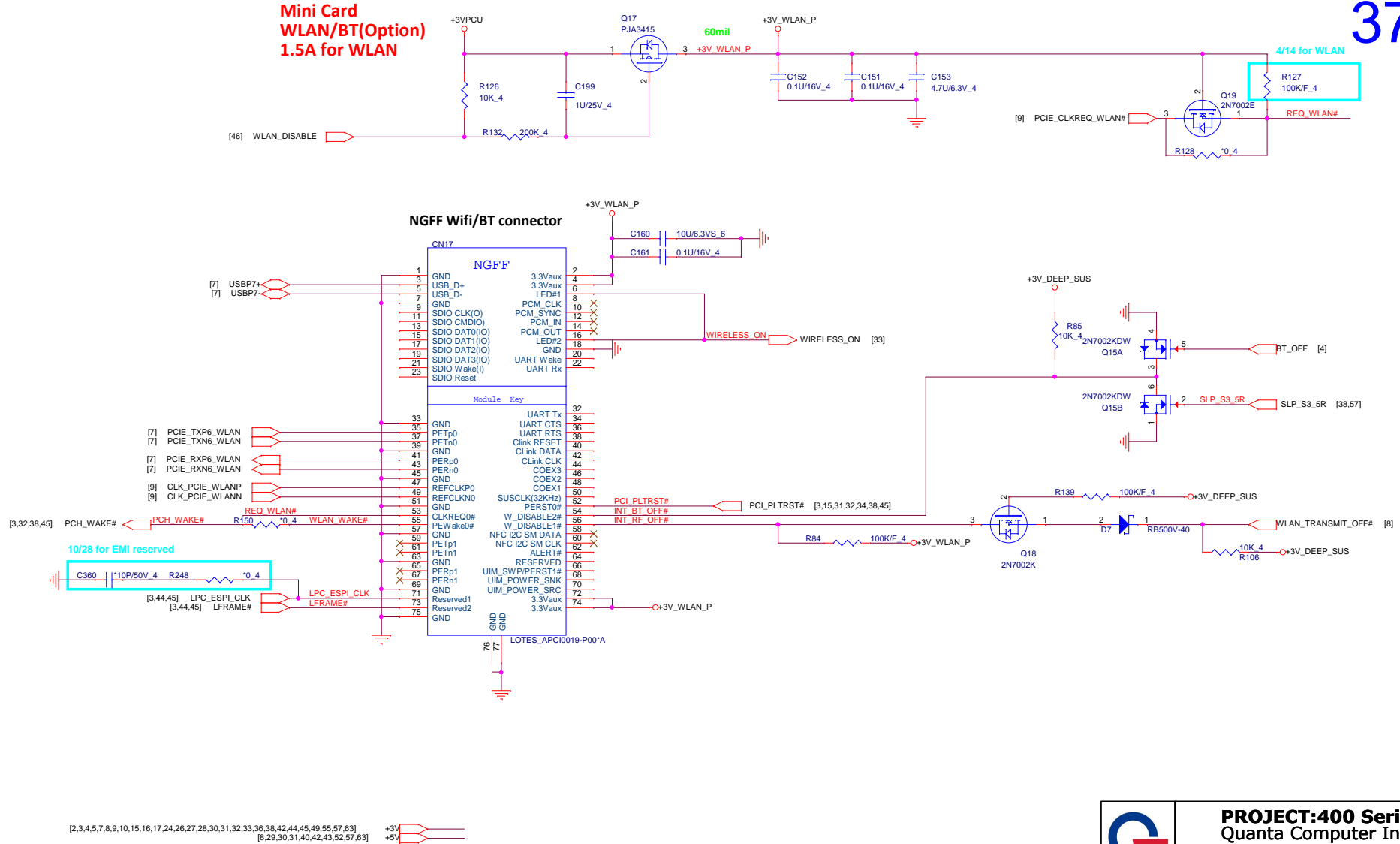


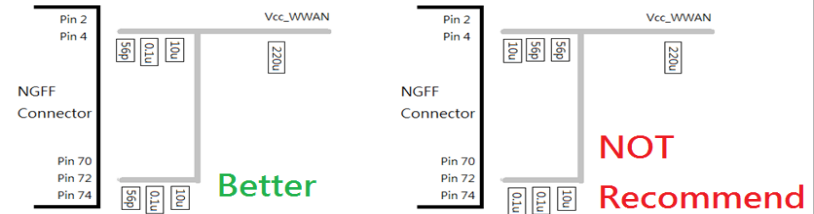
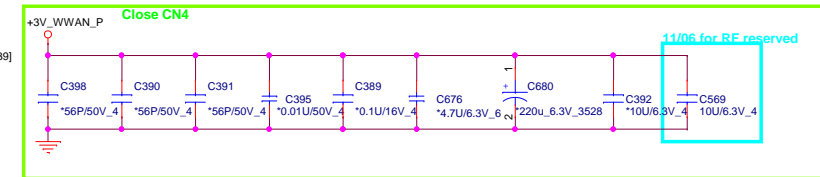
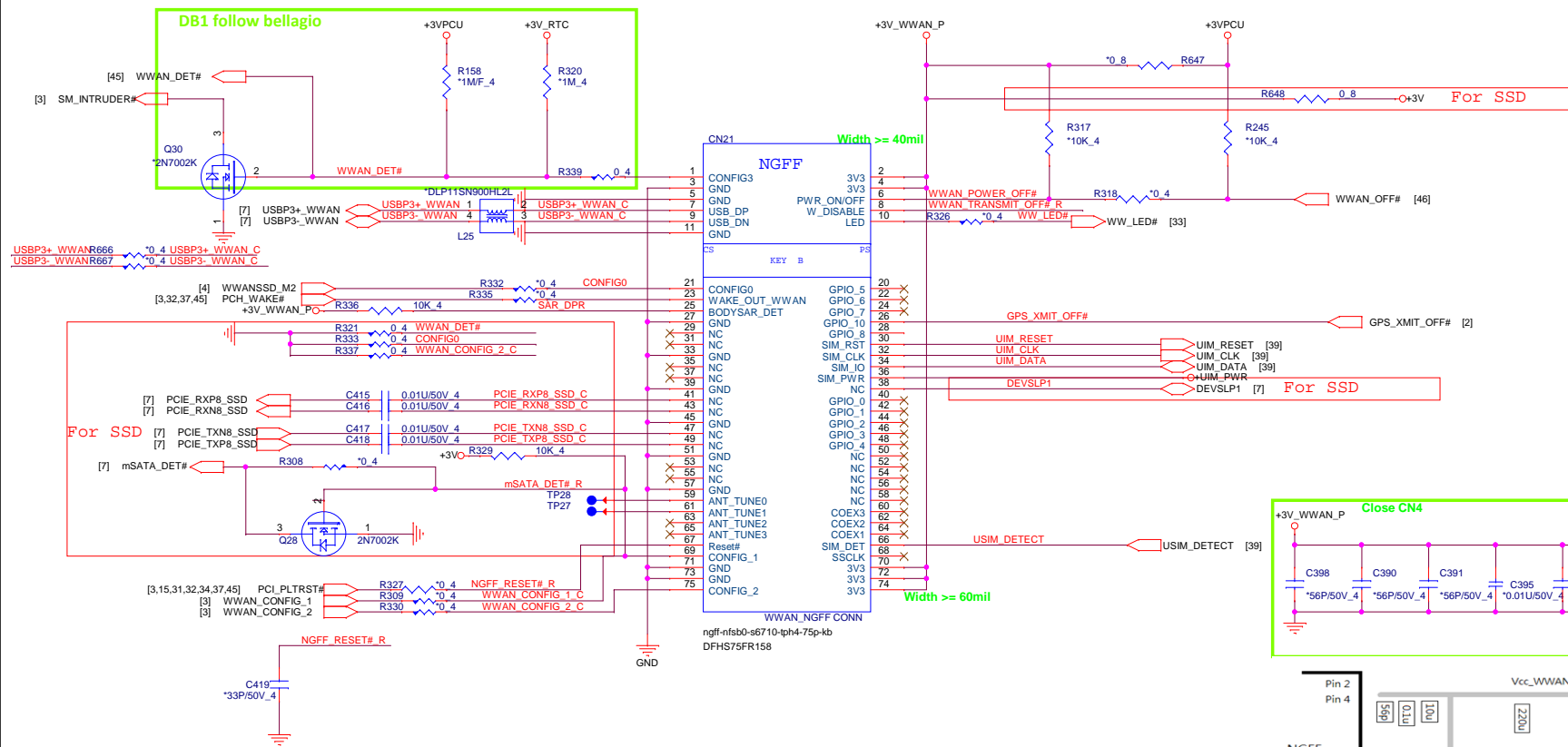
NB5

PROJECT:400 Series
Quanta Computer Inc.

| | | |
|------------------------------|--|-----------|
| Size Custom | Document Number 36 -- TS and Accelerometer | Rev 1A |
| Date: Friday, April 17, 2015 | Sheet 36of | 65 |

Mini Card
WLAN/BT(Optional)
1.5A for WLAN

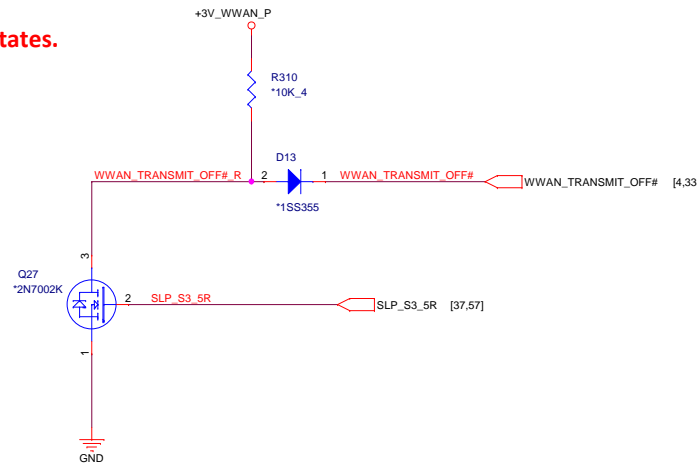




| +VCC | Power_On/Off (Pin6) | W_Disable (Pin8) | GPS_Disable (Pin25) |
|------|---------------------|------------------|---------------------|
| S0 | ON | High | High |
| S3 | ON | High | Low |
| S4 | ON | Low | Low |
| S5 | ON | Low | Low |

WWAN(Optional)
Control of power must be allowed in all S0, S3, S4 and S5 states.

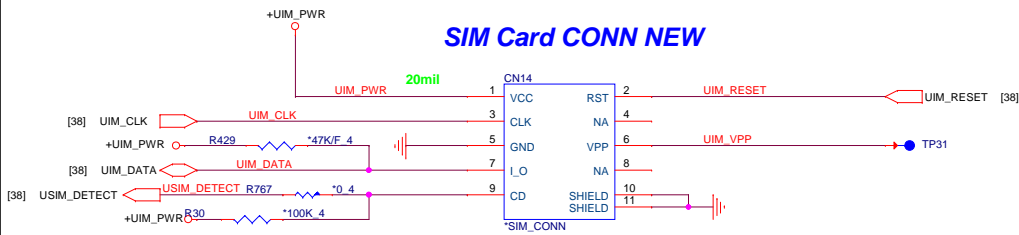
| Pin | M.2 Pinout | S0 | S3 - S5 |
|-----------|------------------|----|---------|
| WWAN 3.3V | 2, 4, 70, 72, 74 | On | Off |



PROJECT:400 Series
Quanta Computer Inc.

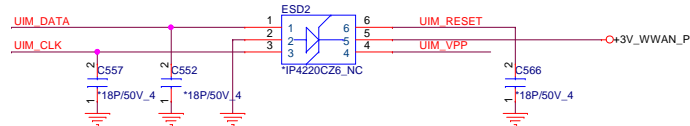
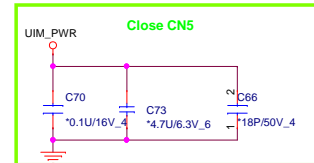
| Size | Document Number | Rev |
|------------------------------|----------------------|-----|
| Custom | 38 -- WWAN NGFF/ SSD | 1A |
| Date: Friday, April 17, 2015 | Sheet 38 of 65 | |

SIM Card CONN NEW



Layout Note:

1. UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible
Route into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances ≥ 2 cm
3. Position the SIM connector from the WWAN module ≤ 100 mm if possible, NOT exceed length is 150mm.

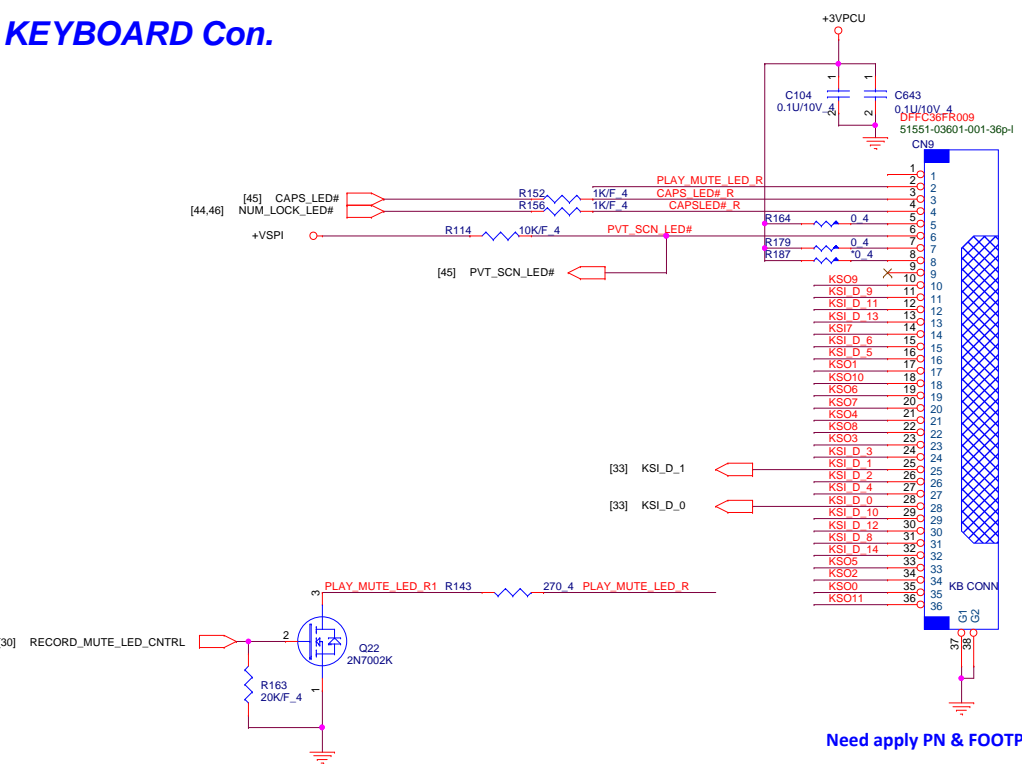
Trace Length and Routing^u

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.^u
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.^u
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.^u
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.^u

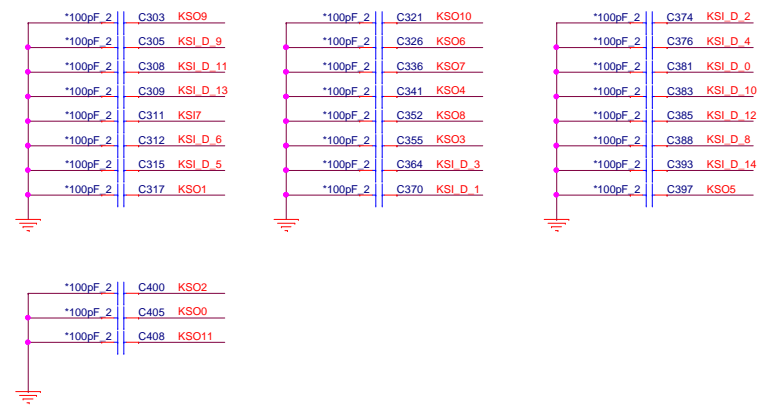
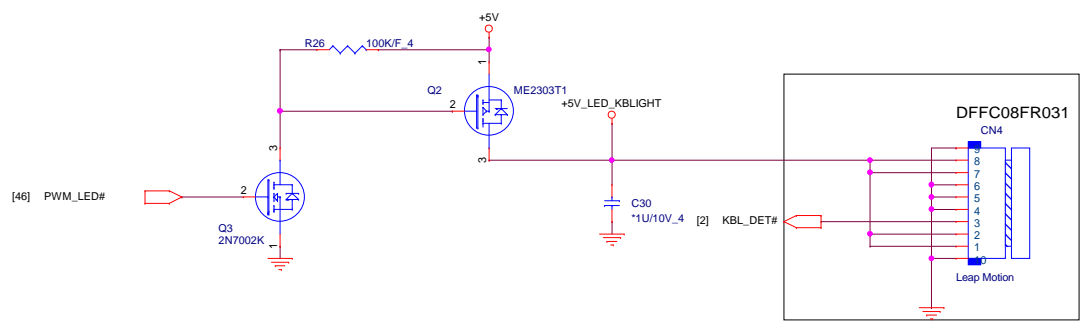
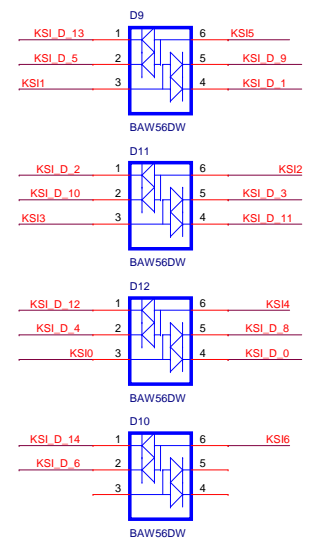
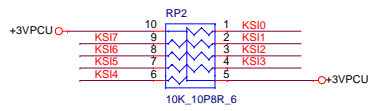
SIM Power^u

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.^u
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.^u

RF cap



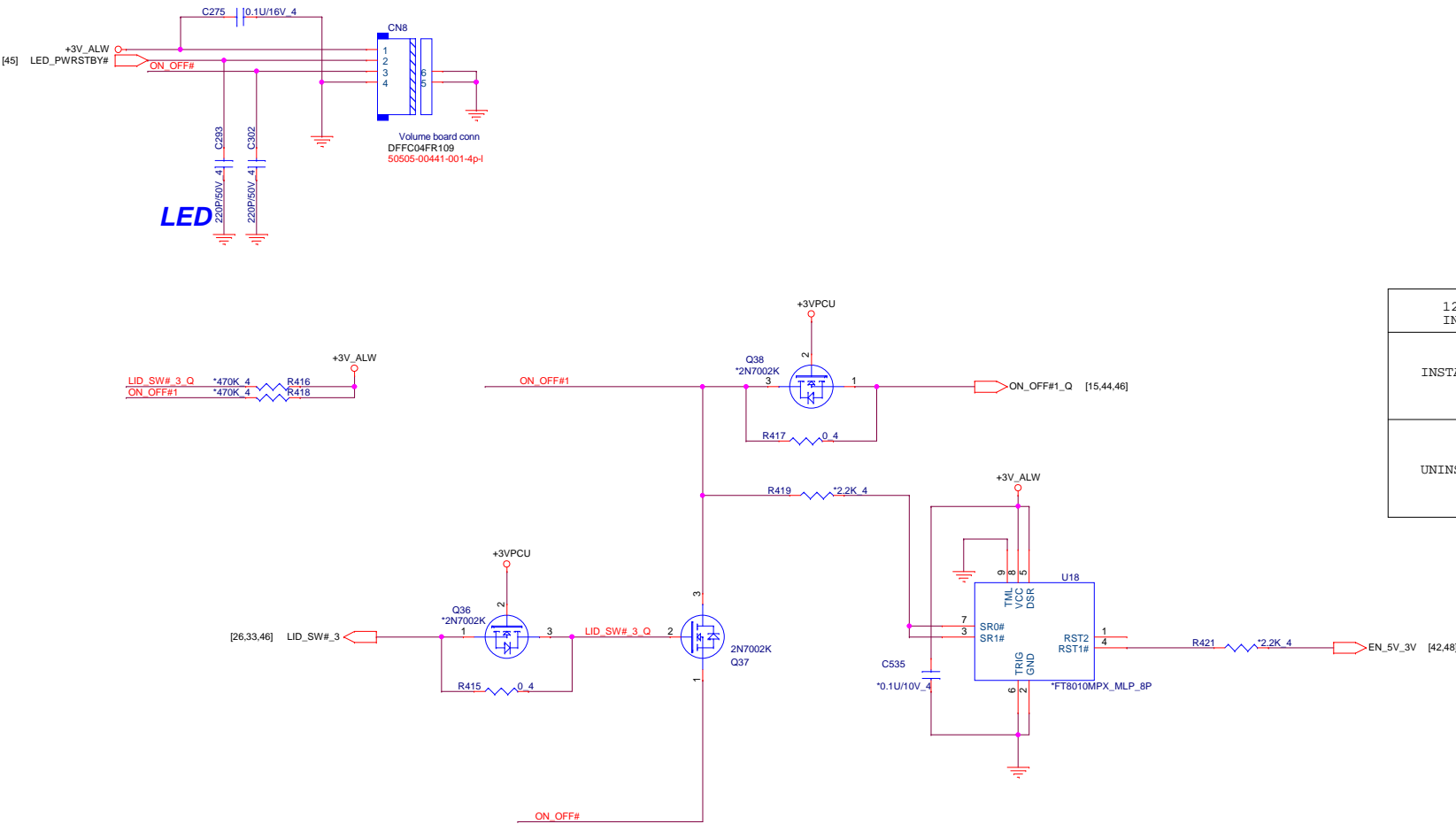
KEYBOARD PULL-UP



[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63]
[8,29,30,31,42,43,52,57,63]


+3V
+5V

Power Botton Connector



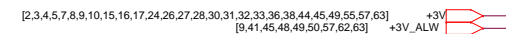
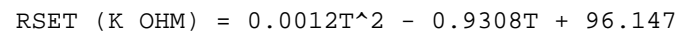
| 12S RESET MODE INSTAL FOR DB0 | | |
|----------------------------------|-------------------------------------|------------------------|
| INSTAL | R10702 R10704 R10701 U9068 | R10703 R581 R595 |
| UNINSTAL | R10754 Q7080 | R10755 Q7081 |

[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63] +3V
[8,29,30,31,40,42,43,52,57,63] +5V
[9,45,48,49,50,57,62,63] +3V_ALW

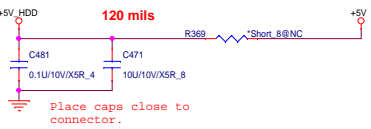
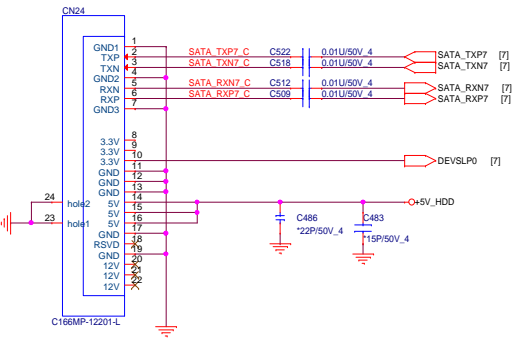


PROJECT:400 Series
Quanta Computer Inc.

| | | |
|------------------------------|---|-----------|
| Size Custom | Document Number 41 - Power Button/ HW Reset | Rev 1A |
| Date: Friday, April 17, 2015 | Sheet 41 of 65 | |



SATA-HDD

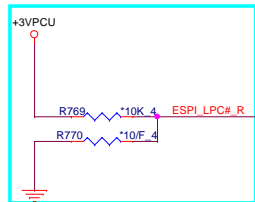


EMI cap

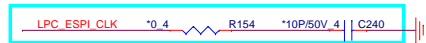
[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,57,63]
[8,29,30,31,40,42,52,57,63]



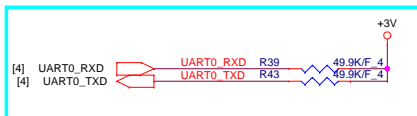
02/10 for Bellagio ESPI



10/28 for EMI reserved



11/04 for check list



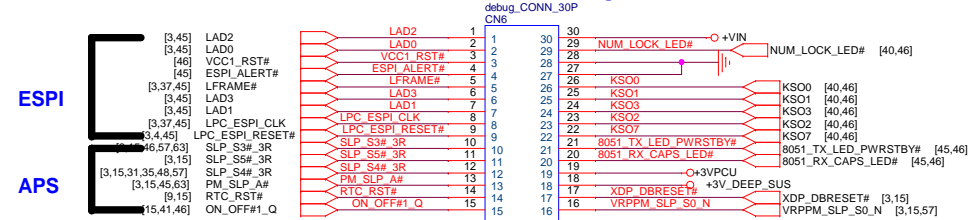
LPC & ESPI TABLE

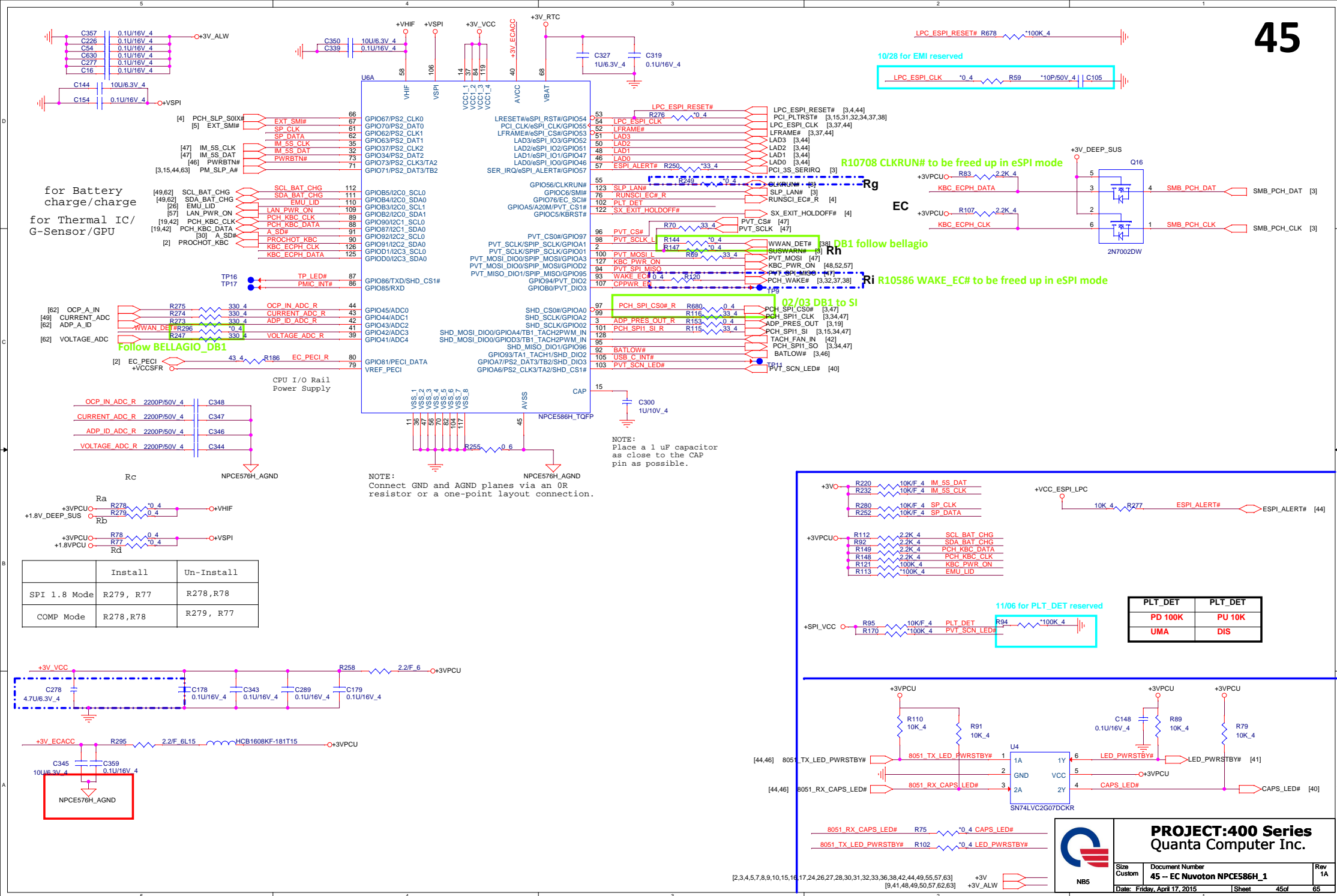
| | LPC MODE | ESPI MODE |
|------|----------|-----------|
| R771 | INSTAL | UNINSTAL |
| R769 | UNINSTAL | INSTAL |
| R770 | INSTAL | UNINSTAL |

LPC & ESPI TABLE

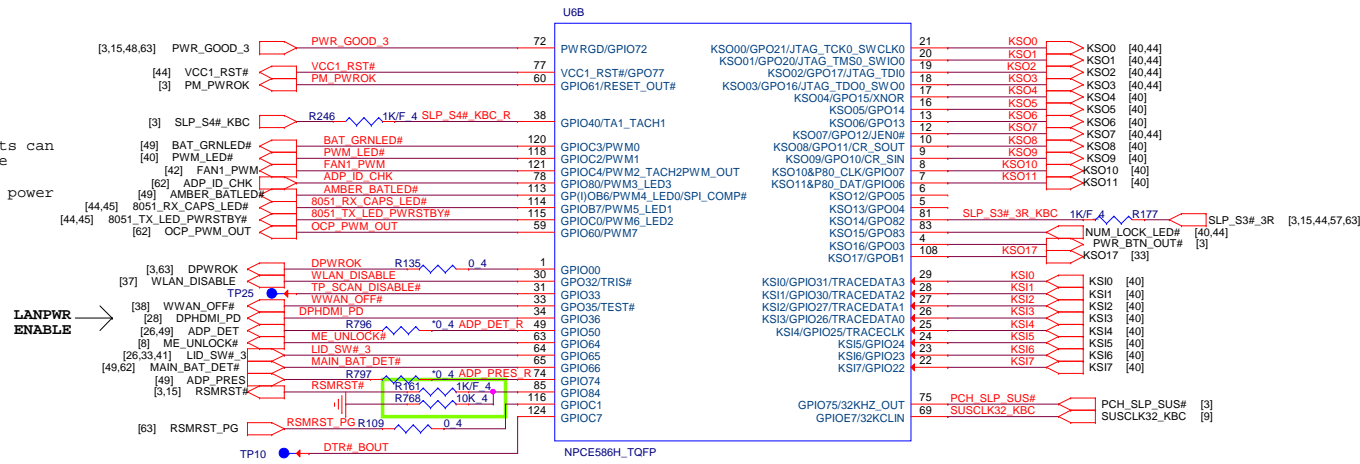
| | LPC MODE | ESPI MODE |
|----------------|----------|-----------|
| R658 Ra | INSTAL | UNINSTAL |
| R646 Rb | INSTAL | UNINSTAL |
| R659 Rc | INSTAL | UNINSTAL |
| R656 Rd | INSTAL | UNINSTAL |
| R649 Re | INSTAL | UNINSTAL |
| R657 Rf | INSTAL | UNINSTAL |
| R249 Rg | INSTAL | UNINSTAL |
| R147 Rh | INSTAL | UNINSTAL |
| R120 Ri | INSTAL | UNINSTAL |
| R276 Rj | INSTAL | UNINSTAL |
| R678 Rk | UNINSTAL | INSTAL |

ESPI+EC+APS debug conn on MB

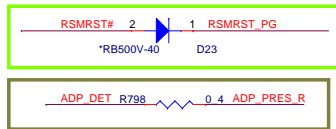




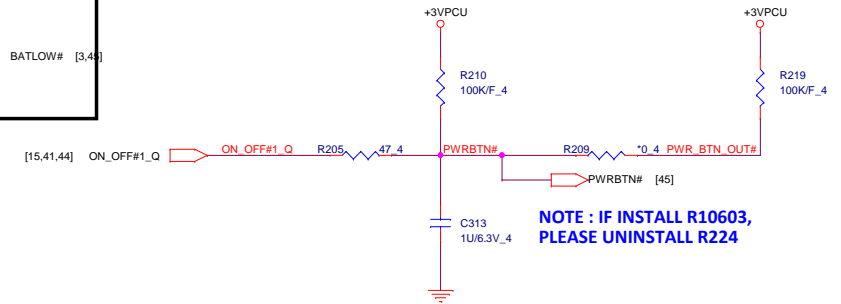
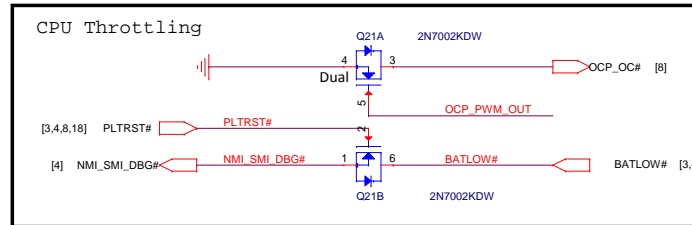
All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power



02/09 for Ji-An suggestions for DB to SI



PV, 0415 add R798 connect ADP_DET and ADPPres_R

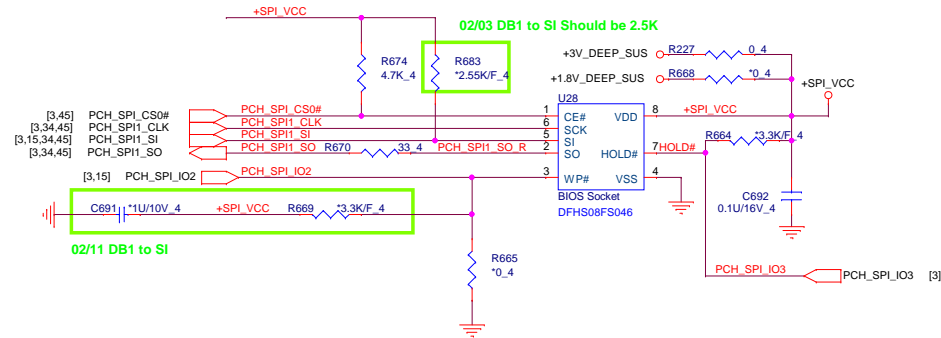
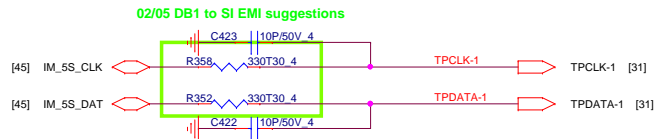
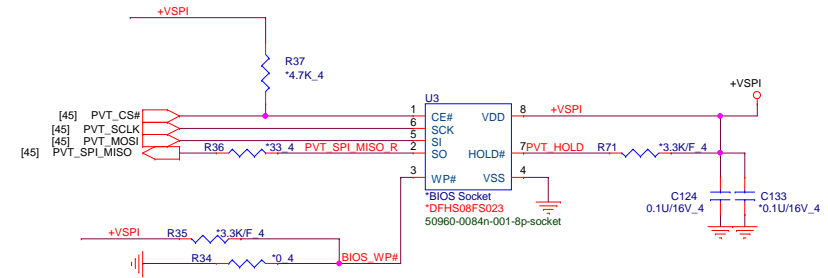


NOTE : IF INSTALL R10603, PLEASE UNINSTALL R224

| Vender | Size | P/N |
|---------|-------|-------------|
| Winbond | 128MB | AKE3DZN0N01 |
| Socket | | DFHS08FS023 |

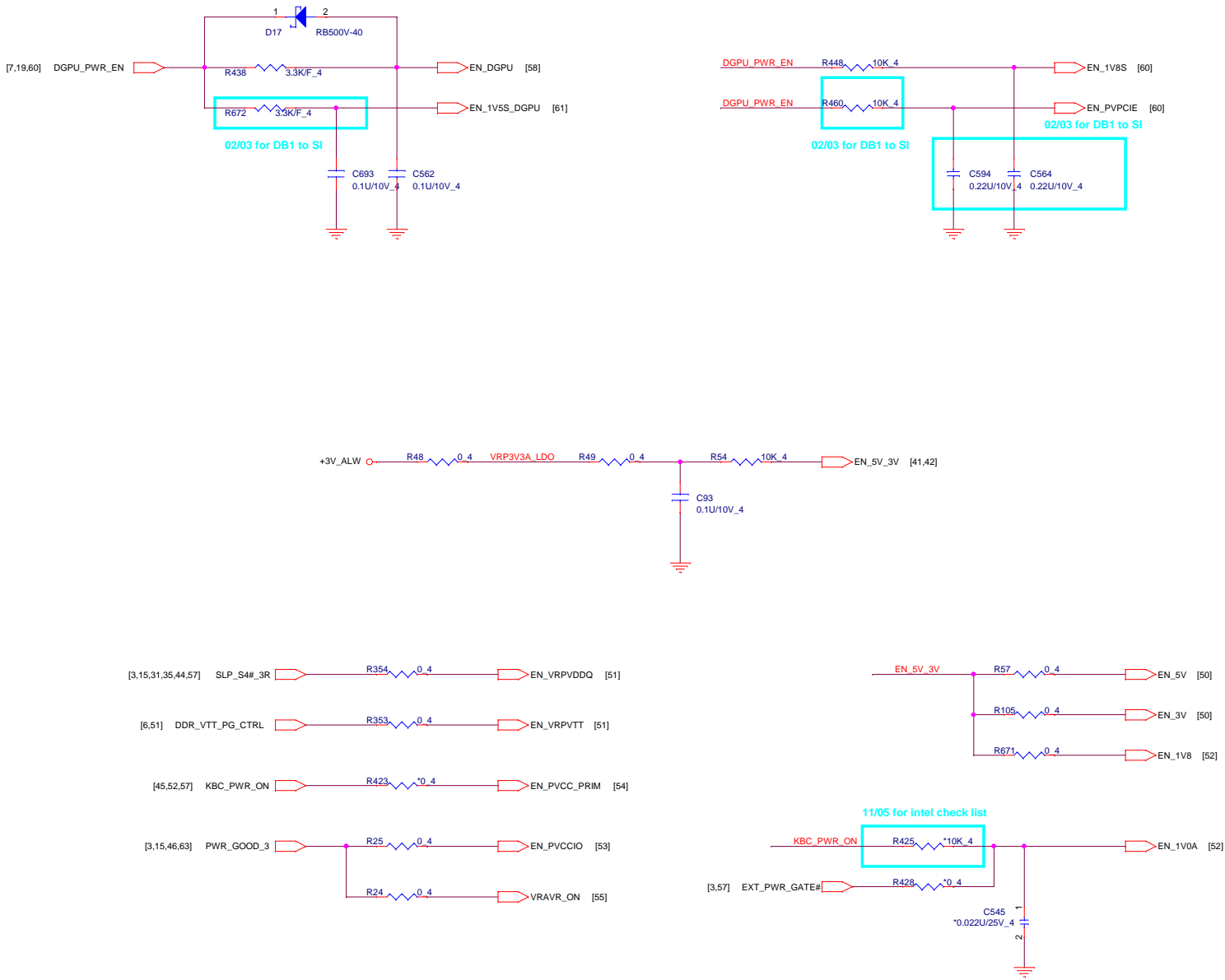
| Vender | Size | P/N |
|---------|------|-------------|
| Winbond | 16MB | AKE38FP0N03 |
| Socket | | DFHS08FS023 |

PCH SPI ROM(CLG)

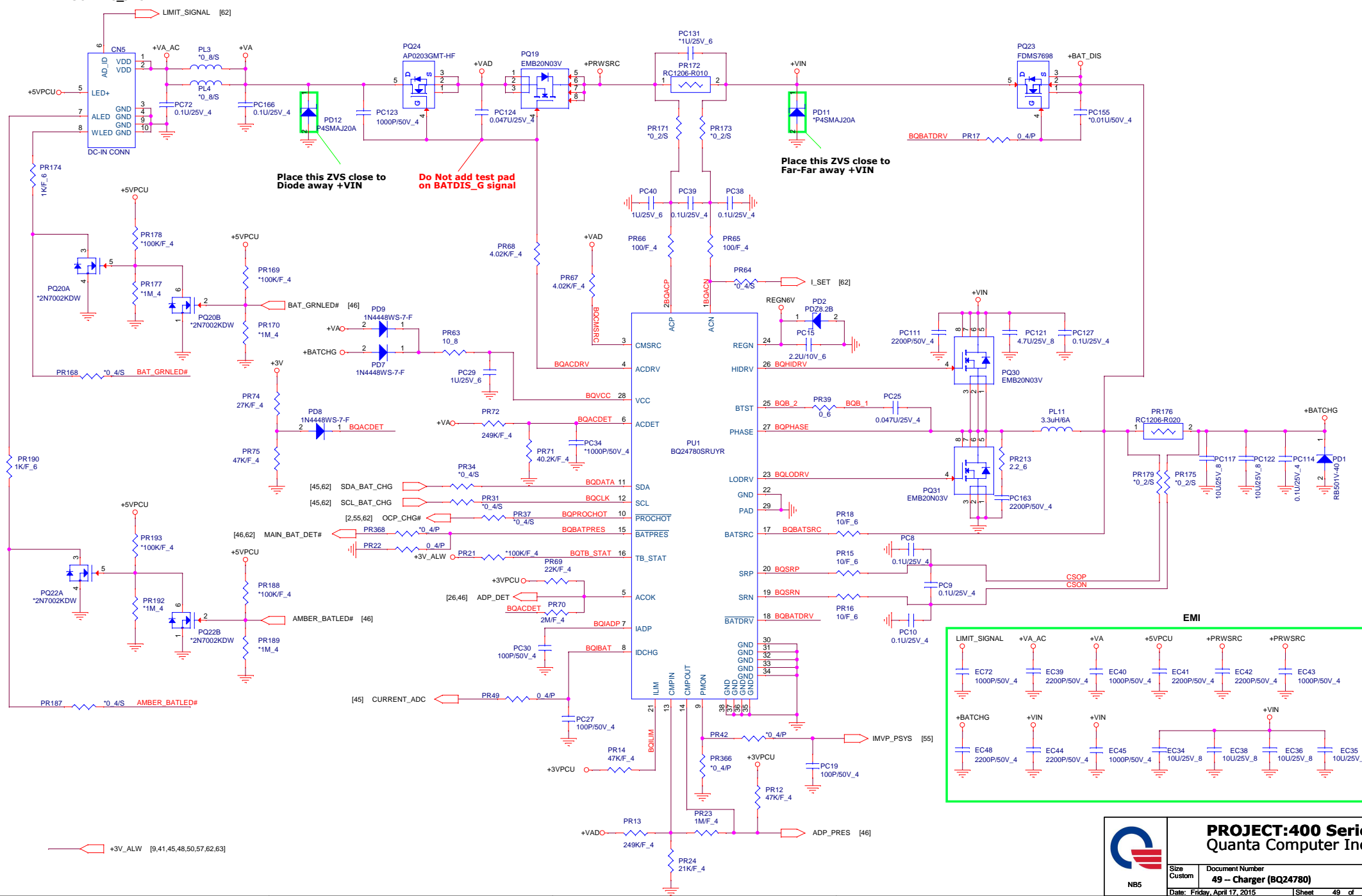
PCH 6*5mm WSON 16M
SPI ROM SocketEC 6*5mm WSON 8M
SPI ROM Socket

400 series 1001

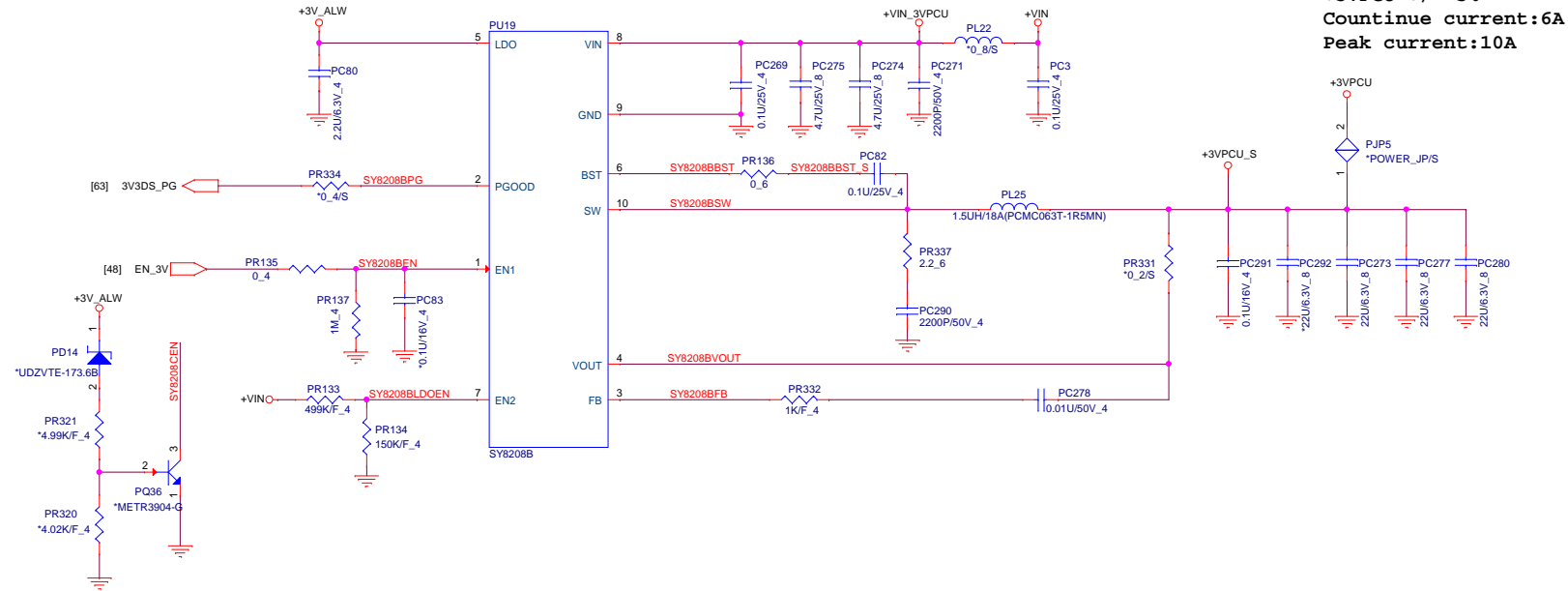
POWER TO EE NET NAME CONNECTION



90W DC JACK

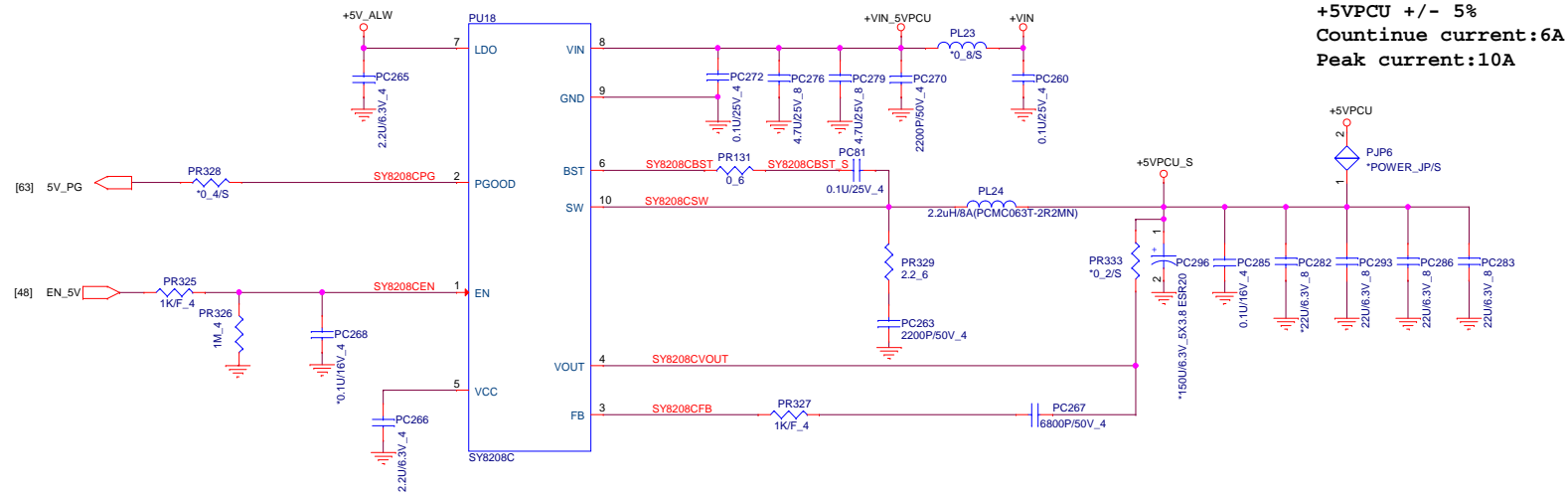


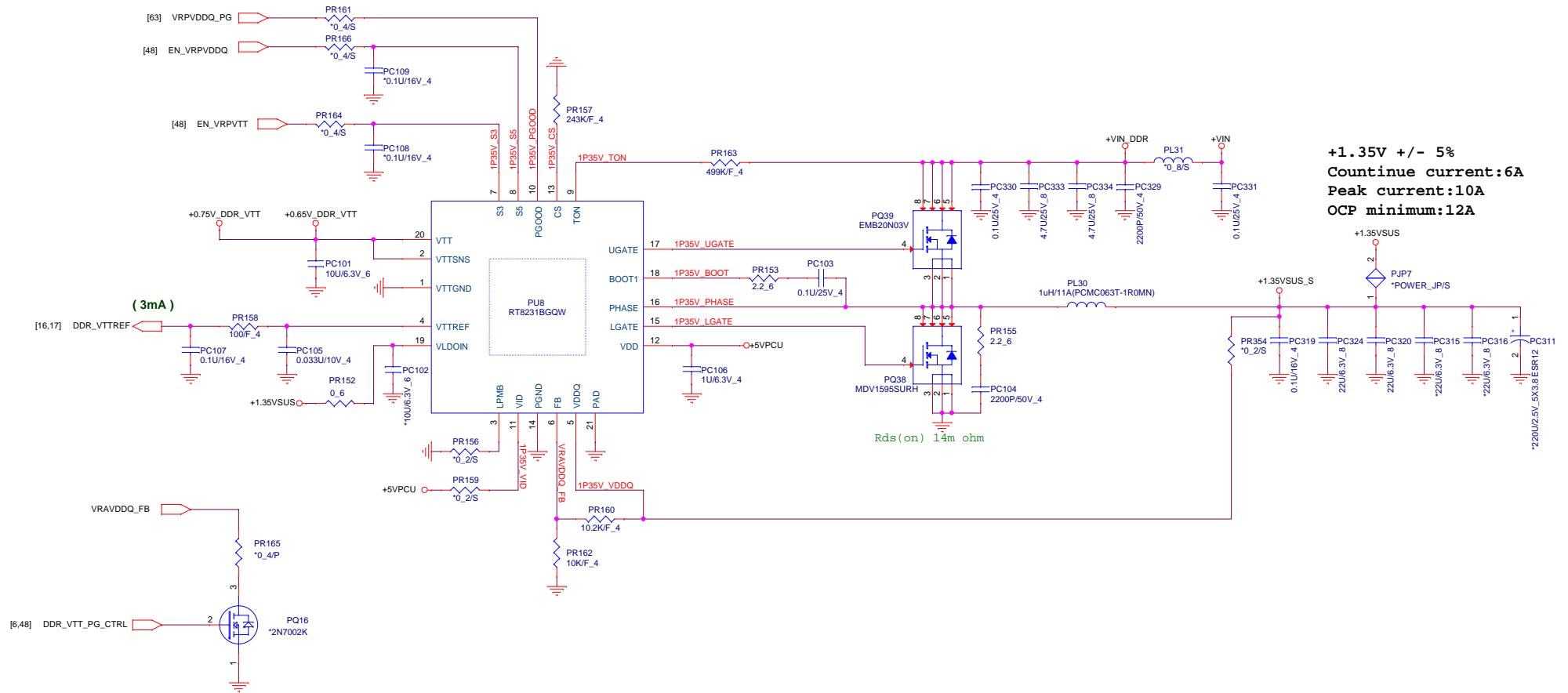
Do Not add test pad
on +3VPCU



+3VPCU [3,10,15,26,33,37,38,40,41,42,44,45,46,49,53,54,57,60,62,63]
+5VPCU [31,35,49,51,52,55,56,57,58,60,61,63]

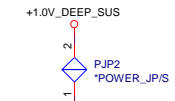
Do Not add test pad
on +5VPCU




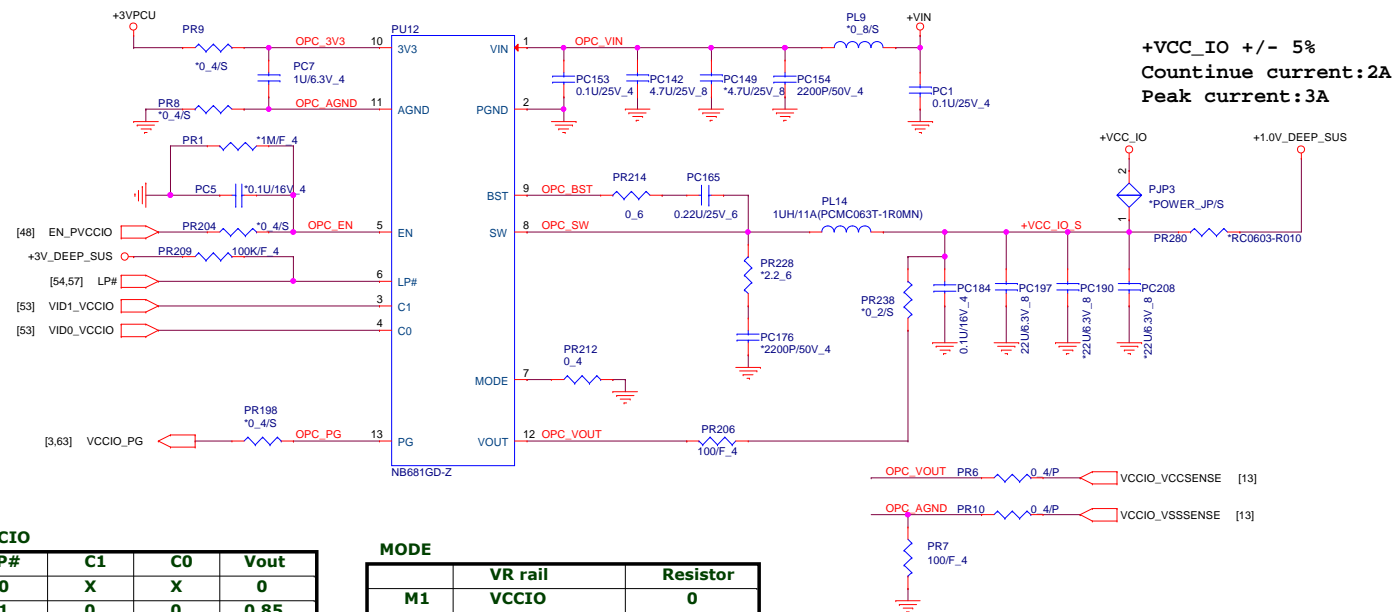
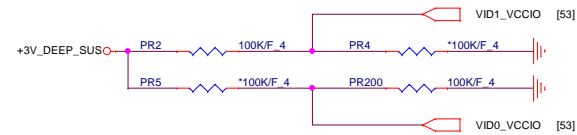
 +1.35VSUS [6,13,16,17]

PROJECT:400 Series
Quanta Computer Inc.

| | | |
|-------|--|----------------|
| Size | Document Number 51 – DDR3 (RT8231B) | Rev 1A |
| Date: | Friday, April 17, 2015 | Sheet 51 of 65 |



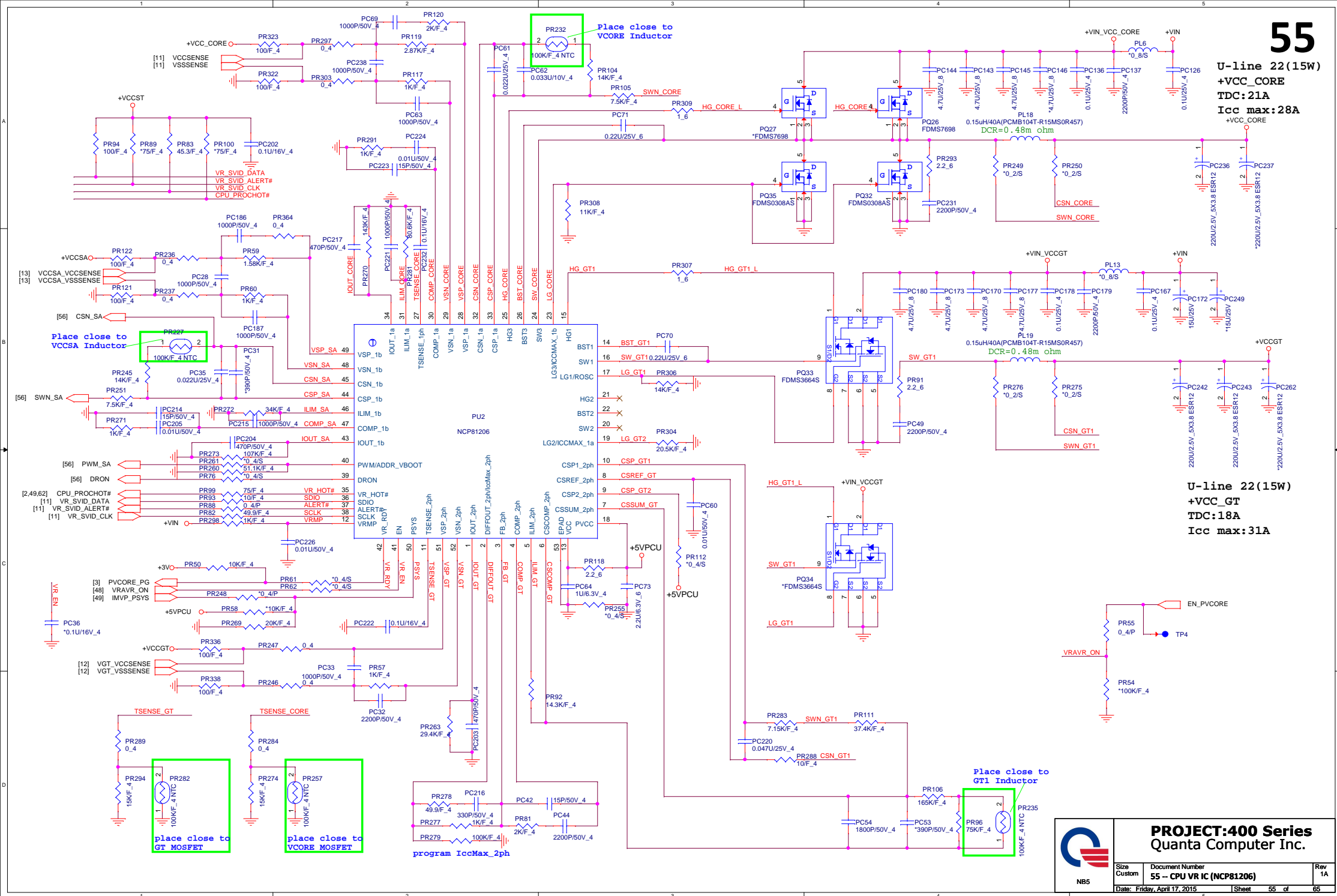
| | | | |
|--|---|---|----------------|
|  NB5 | PROJECT:400 Series Quanta Computer Inc. | | |
| | Size | Document Number 52 -- +1.0VSS/1.8VSS | Rev 1A |
| | Date: | Friday, April 17, 2015 | Sheet 52 of 65 |

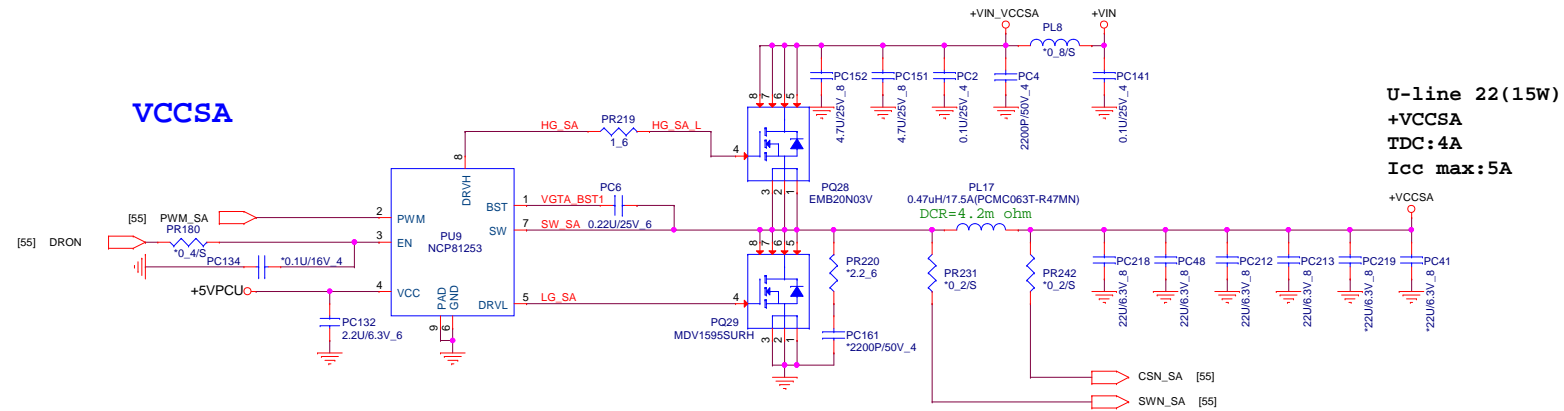


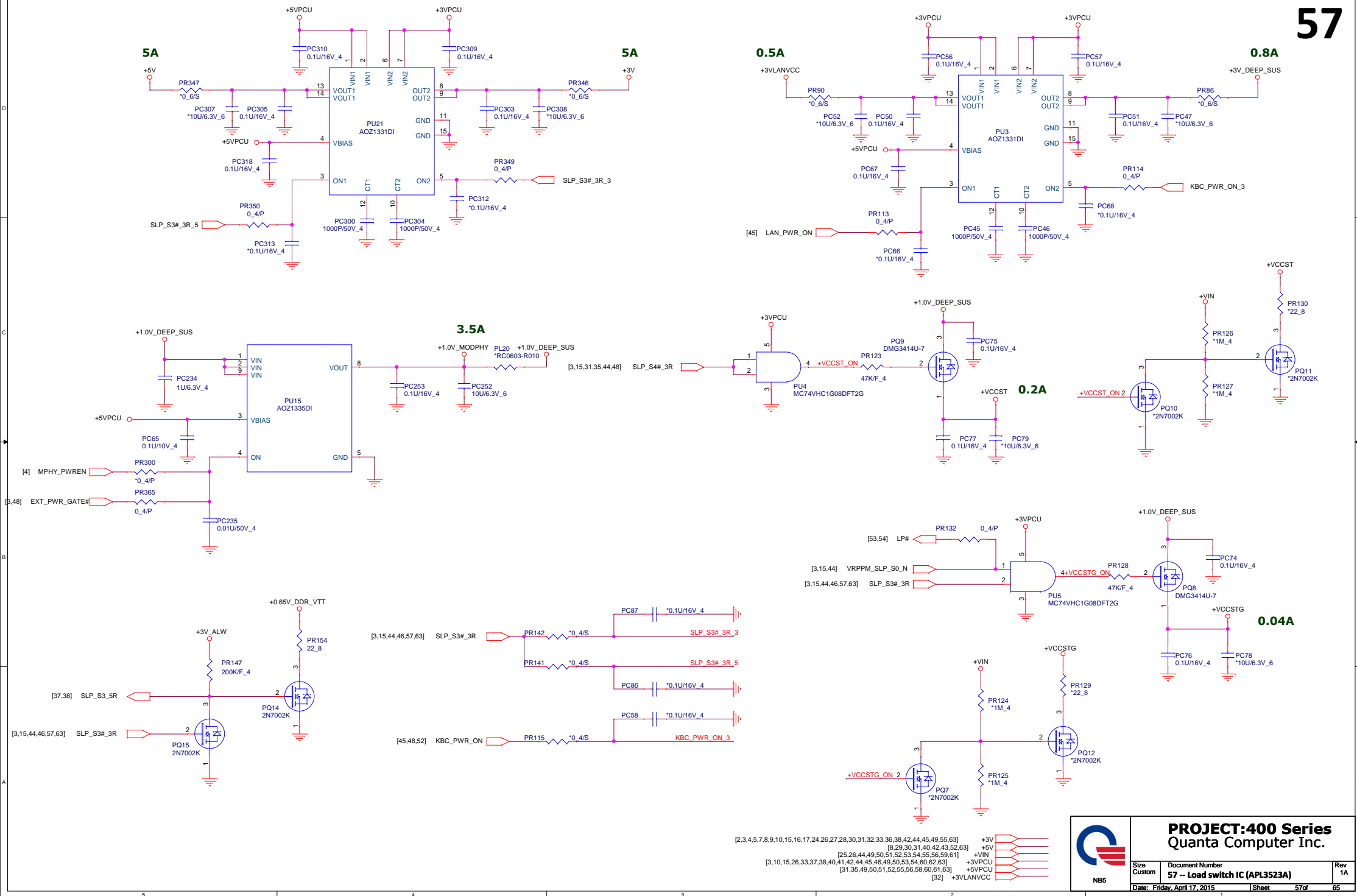
| VCCIO | | | |
|-------|----|----|-------|
| LP# | C1 | C0 | Vout |
| 0 | X | X | 0 |
| 1 | 0 | 0 | 0.85 |
| 1 | 0 | 1 | 0.875 |
| 1 | 1 | 0 | 0.95 |
| 1 | 1 | 1 | 0.975 |

| MODE | | |
|------|--------------|----------|
| | VR rail | Resistor |
| M1 | VCCIO | 0 |
| M2 | PRIMCORE | Float |
| M3 | EDRAM/EOPPIO | 100K |
| M4 | other | 150K |


U-line 22(15W)
+VCC_CORE
TDC:21A
Icc max:28A

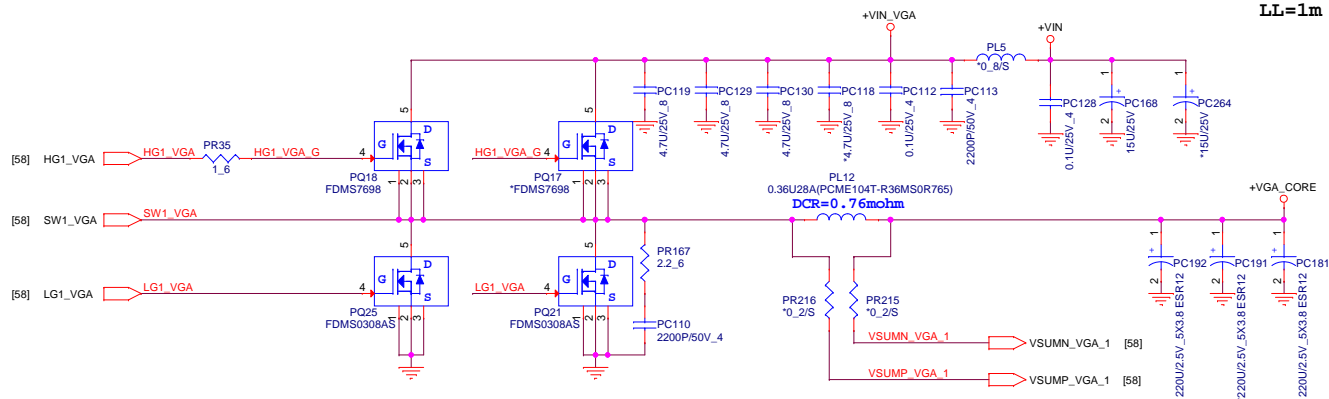


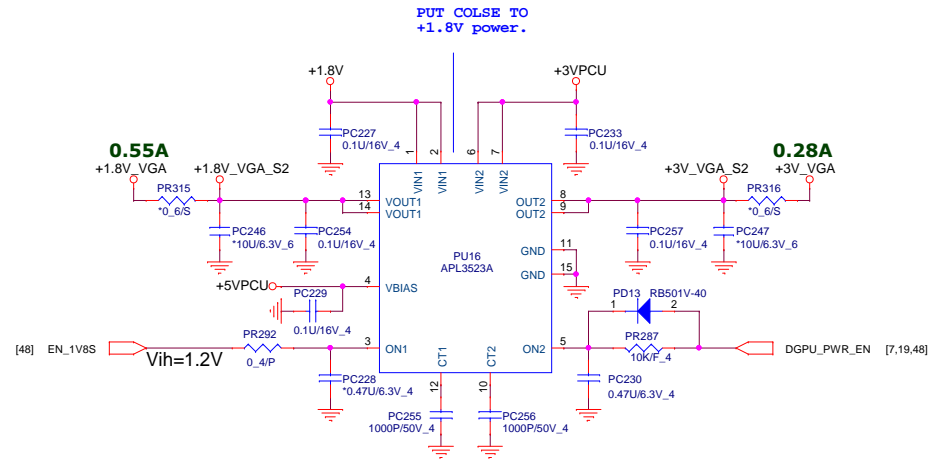
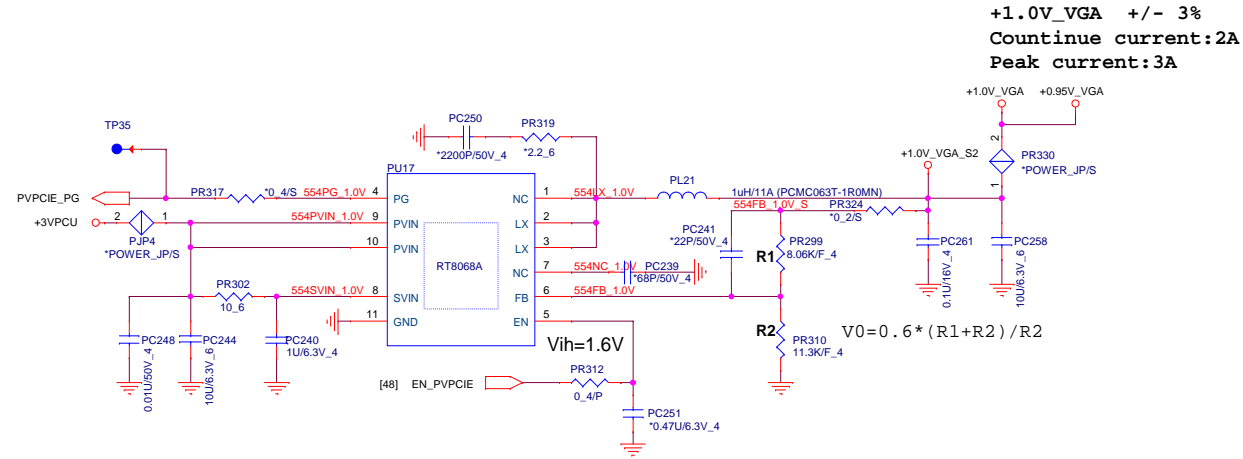


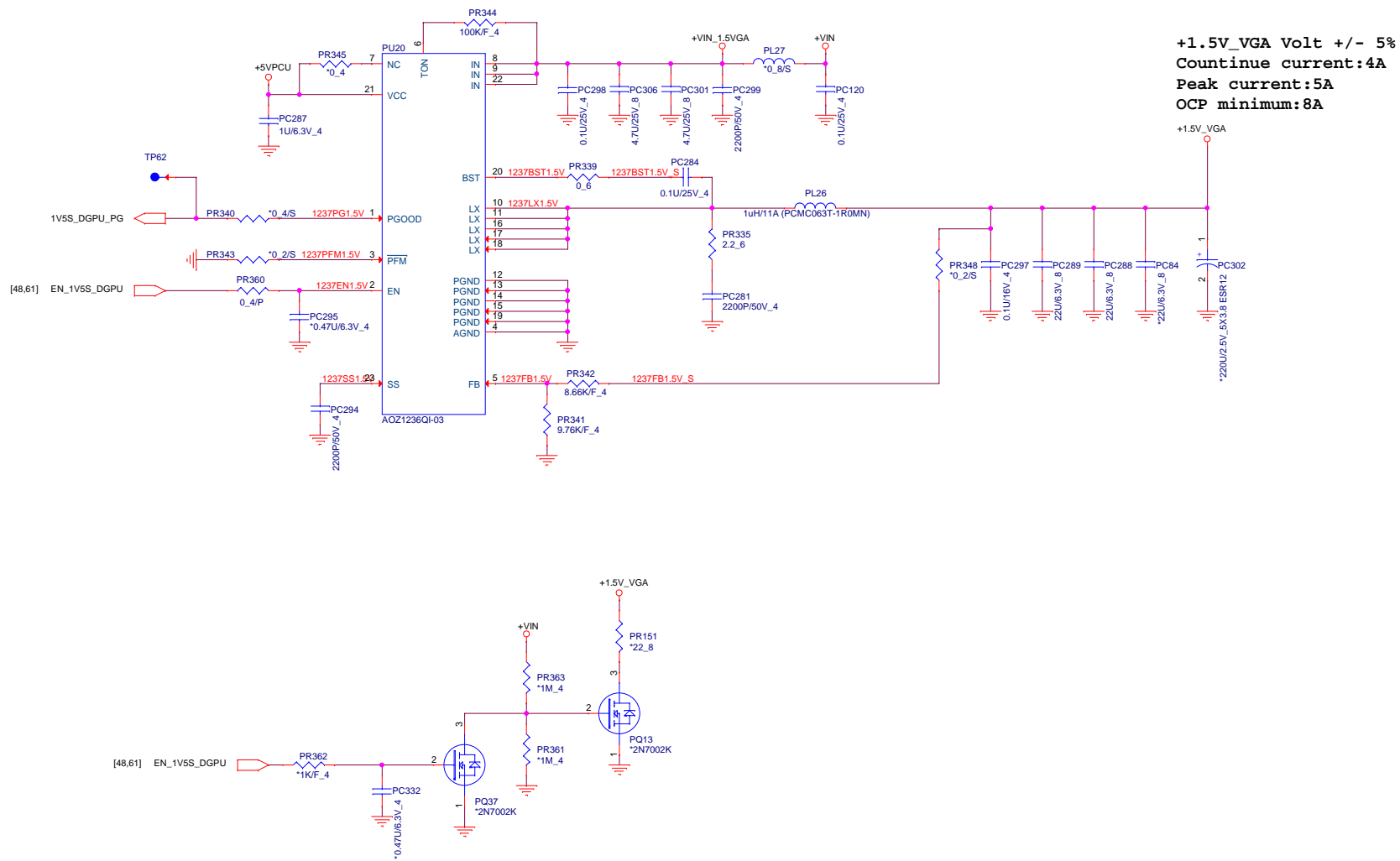


[2,3,4,5,7,8,9,10,15,16,17,24,26,27,28,30,31,32,33,36,38,42,44,45,49,55,63]
 [8,29,30,31,40,42,43,52,63]
 [25,26,44,49,50,51,52,53,54,55,56,59,61]
 [3,10,15,26,33,37,38,40,41,42,44,45,46,49,50,53,54,60,62,63]
 [31,35,49,50,51,52,55,56,58,60,61,63]
 [32] +3VLANVCC

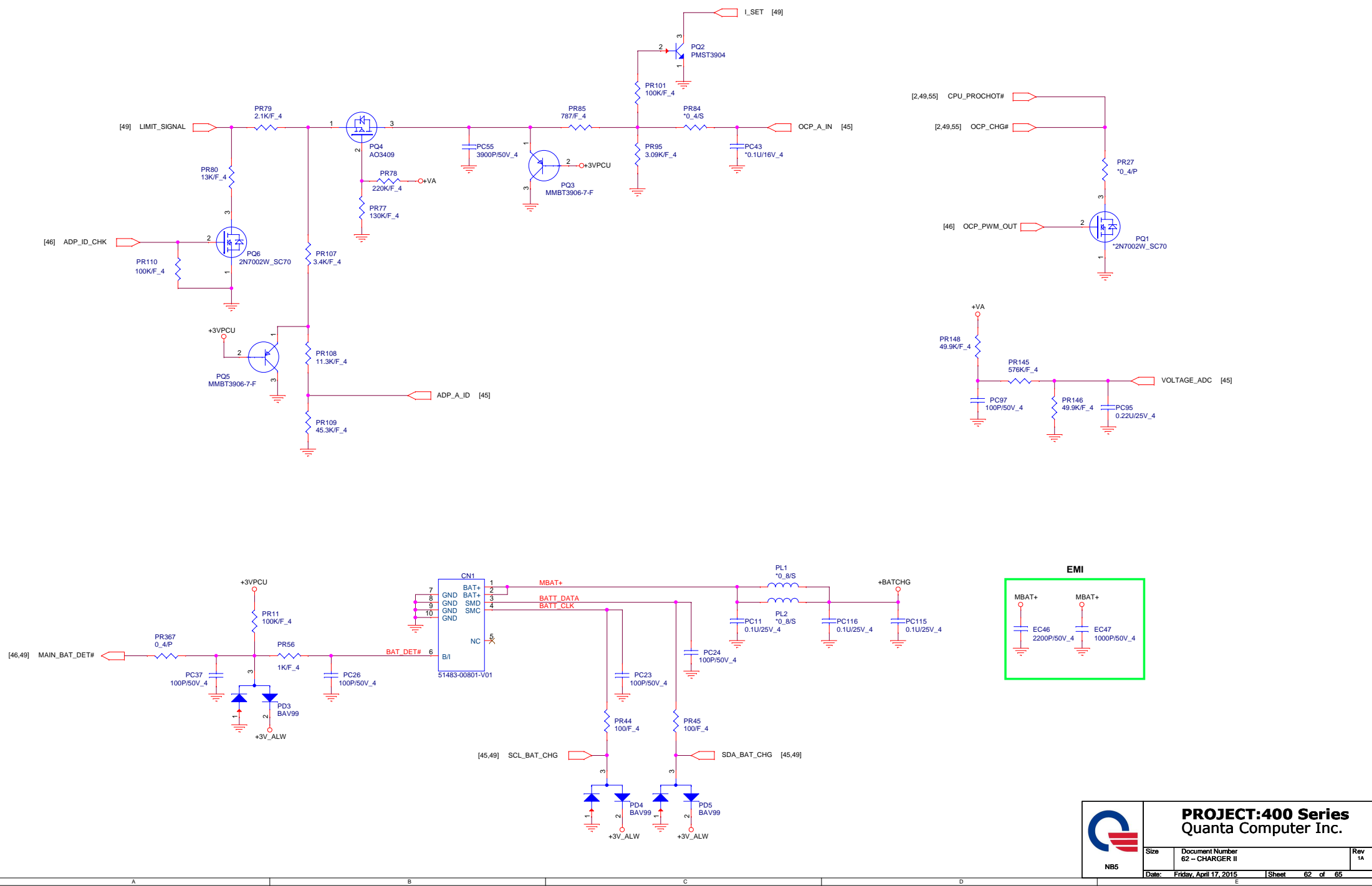
| | | | |
|---|--|--|--------|
|  | PROJECT:400 Series Quanta Computer Inc. | | |
| | Size Custom | Document Number 57 – Load switch IC (APL3523A) | Rev 1A |
| Date: Friday, April 17, 2015 | Sheet 57 of 65 | | |





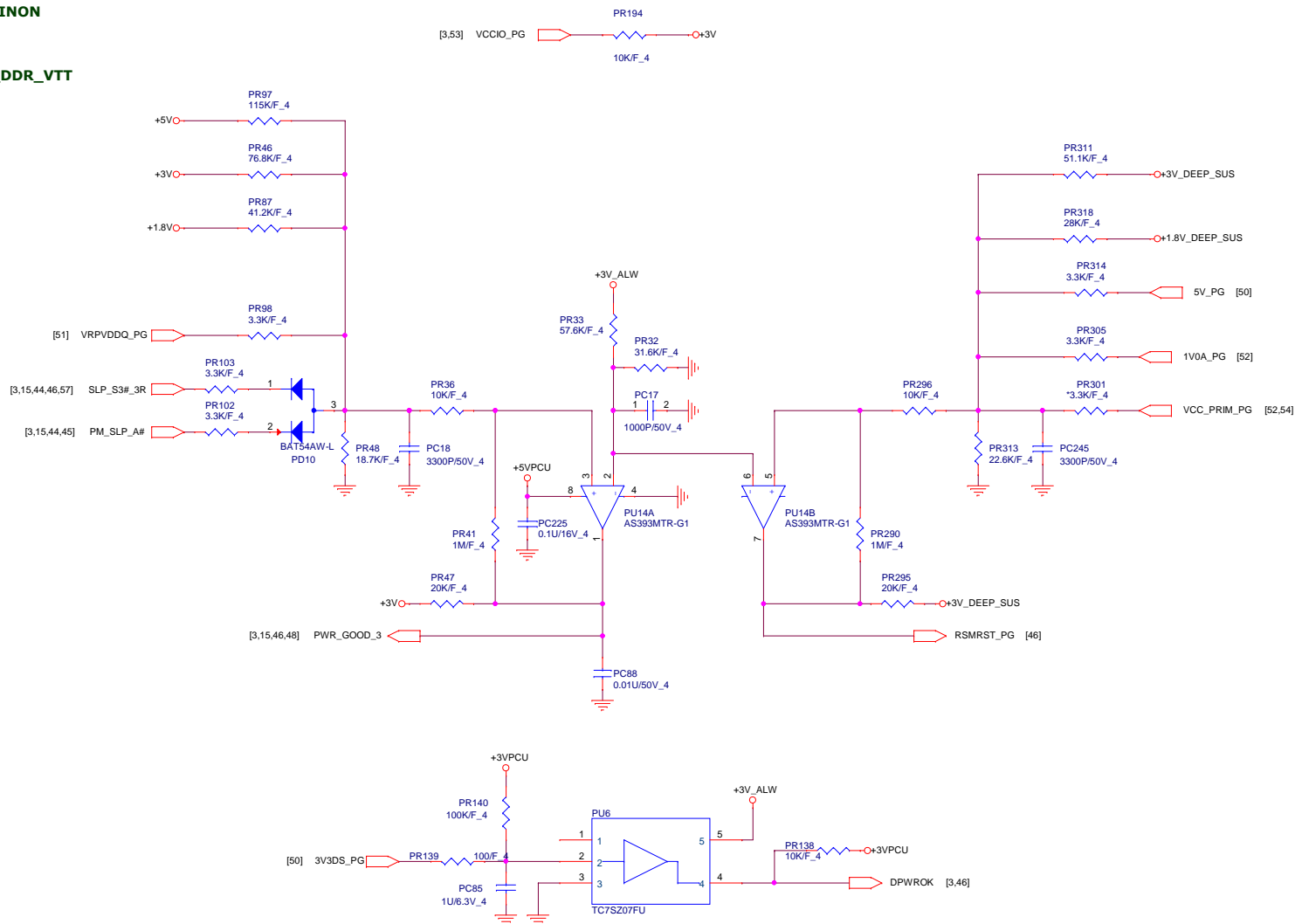


Adapter OCP

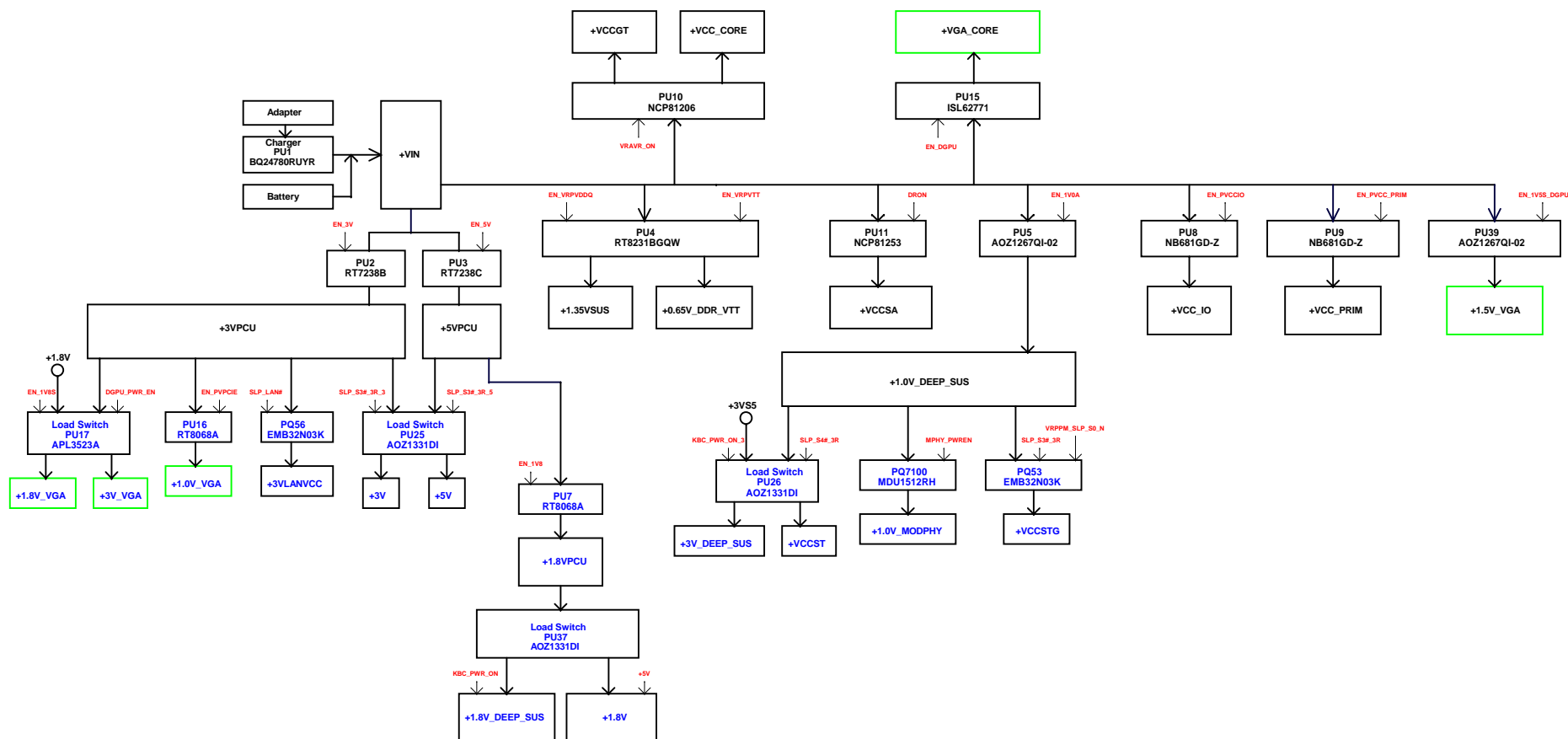


POK CKT

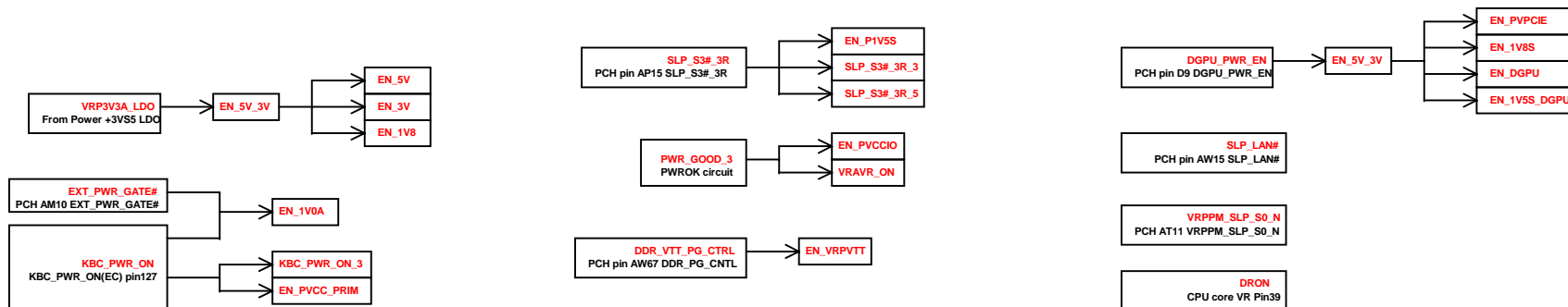
```
PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S = +0.75V_DDR_VTT
```



POWER BLOCK DIAGRAM

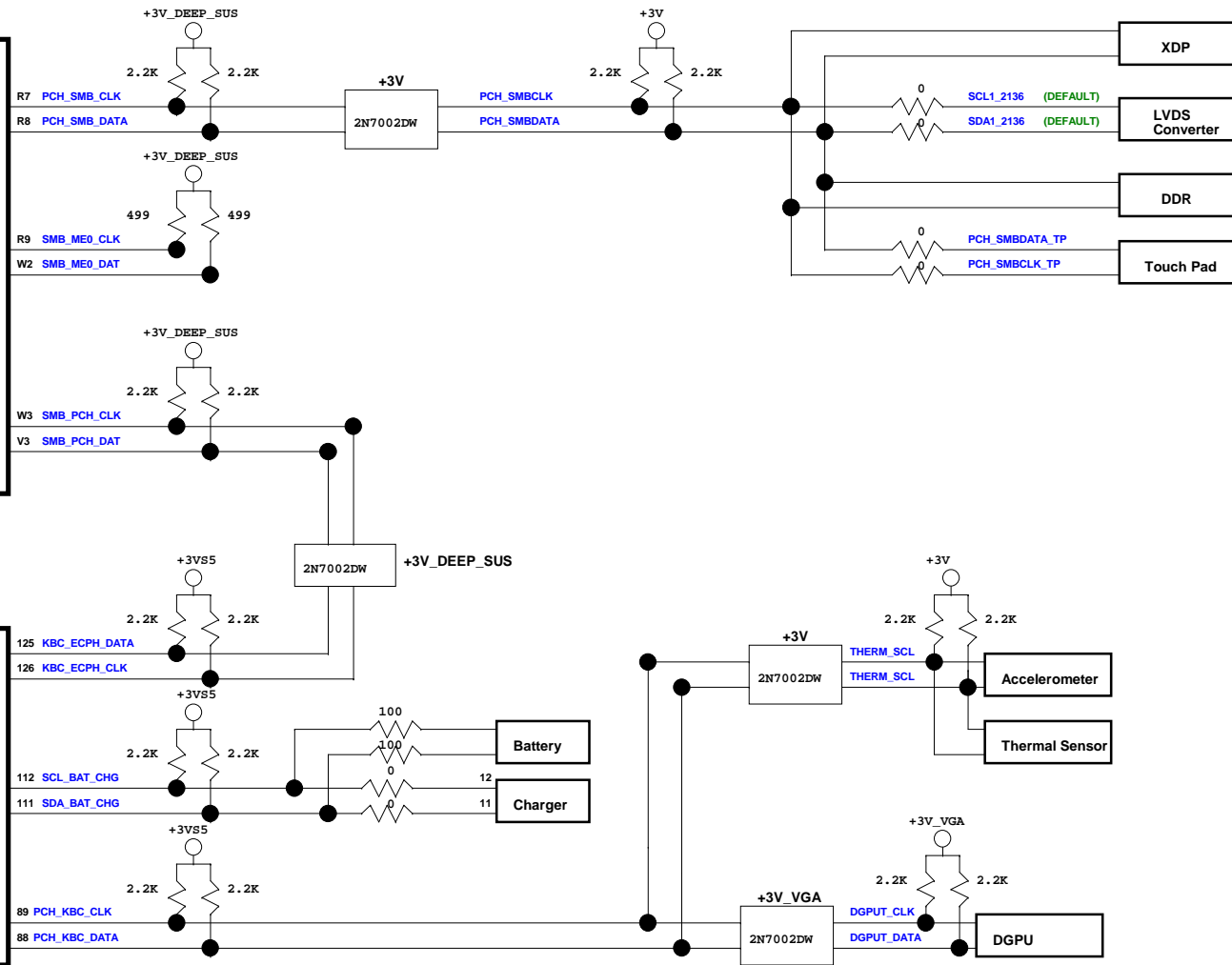


POWER ENABLE PIN



SKYLAKE U

EC
NPCE586H



Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

| Multiplexed HSIO Lane | Port Assignment |
|-----------------------|--|
| USB3 #1 | USB2.0/USB3.0 Combo Jack(Left side down) |
| USB3 #2 / SSIC #1 | USB2.0/USB3.0 Combo Jack(Left side up) |
| USB3 #3 / SSIC #2 | NC |
| USB3 #4 | NC |
| PCIE1 / USB3 #5 | dGPU |
| PCIE2 / USB3 #6 | dGPU |
| PCIE3 | dGPU |
| PCIE4 | dGPU |
| PCIE5 | LAN |
| PCIE6 | WLAN |
| PCIE7 / SATA #0 | HDD (SATA) |
| PCIE8 / SATA #1 | ODD (SATA) |
| PCIE9 | Cardreader (PCIE) |
| PCIE10 | NC |
| PCIE11 / SATA #1* | NC |
| PCIE12 / SATA #2 | SSD (SATA) |

| USB2.0 | Port Assignment |
|----------|--|
| USB2 #1 | USB2.0/USB3.0 Combo Jack(Left side down) |
| USB2 #2 | USB2.0/USB3.0 Combo Jack(Left side up) |
| USB2 #3 | WWAN |
| USB2 #4 | USB2.0(Right side on USB Board) |
| USB2 #5 | USB2.0(Right side on USB Board) |
| USB2 #6 | Touch Screen |
| USB2 #7 | Bluetooth |
| USB2 #8 | Finger Print |
| USB2 #9 | Camera |
| USB2 #10 | NC |